Acromag®

Series 9440/9443/9447

Isolated Digital I/O Board

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ redundancy, and comprehensive failure analysis to insure a safe and satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

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TABLE OF CONTENTS

CHAPTER

TABLE OF CONTENTS

CHAPTER

FIGURES:

APPENDIX:

1.0 GENERAL INFORMATION

1.1 INTRODUCTION

The AVME944x Series of VME cards offer a variety of features which make them an ideal choice for many industrial and scientific applications.

MODEL	16 Channel Digital In	16 Channel Digital Out	Channel On LEDs
AVME9440-I	XX	XX	
AVME9440-I-L	XX	XX	XX
AVME9443-I		XX	
AVME9443-I-L		XX	XX
AVME9447-I	XX		
AVME9447-I-L	XX		XX

General Features

- All Digital Inputs and Outputs are optically isolated from the VMEbus and from each other (250 VAC).
- Field connections accessible through connectors mounted on the Front Panel.
- Can be interfaced to TTL & CMOS logic.
- PASS/FAIL status indicator LEDs on the front panel.
- Optional Termination Panels.

1.2 DIGITAL INPUT FEATURES (9440-I & 9447-I)

- 16 input points configured as a 16 bit word.
- Input range of up to 55 VDC (over 2 selectable ranges).
- Optically-coupled logic gates.
- Adjustable debounce circuitry.
- Generation of interrupts for channels 0 through 7: input Change Of State (COS), input level (polarity) match, or input pattern detection.
- Input channel ON indicating LEDs (with -L option).

1.3 DIGITAL OUTPUT FEATURES (9440-I & 9443-I)

- 16 output points configured as a 16 bit word.
- Ability to read back output states (for complete confidence in the output setting, the output should be fed back to an input point and the input point monitored).
- Outputs sink up to 1 Amp DC, from up to a 55 VDC source.
- Solid State Relays (SSRs) operate as Single Pole, Single Throw (SPST), Form A relays.
- Output channel ON (output switch closed) indicating LEDs (with -L option).

1.4 VMEbus INTERFACE FEATURES

- Slave module A24/A16, D16/D08 (EO).
- Short I/O Address Modifiers 29H, 2DH (H = Hex).
- Standard Address Modifiers 39H, 3DH (H = Hex).
- I(1-7) interrupter, jumper programmable interrupt level, software programmable interrupt vectors (for digital input channels 0-7), interrupt release mechanism is Release On Register Access (RORA) type.
- Decode on 1K byte boundaries.

1.5 FIELD COMPATIBILITY

See APPENDIX A for more information on compatible products.

1.5.1 Digital Inputs

Directly compatible with Acromag input termination panel.

Cable:

Model 9944-X: Flat 64 pin cable (female connectors at both ends) for connecting the AVME944X to the 6985-16DI termination panel.

Termination Panel:

Model 6985-16DI: Sixteen channel input digital termination panel.

1.5.2 Digital Outputs

Directly compatible with Acromag output termination panel.

Cable:

Model 9944-X: Flat 64 pin cable (female connectors at both ends) for connecting the AVME944X to the 6985-16DO termination panel.

Termination Panel:

Model 6985-16DO: Sixteen channel output digital termination panel.

2.0 PREPARATION FOR USE

This chapter provides information about preparing the Isolated Digital I/O Board for system operation.

2.1 UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

The board is physically protected with foam and electrically protected with an antistatic bag during shipment. It is advisable to visually inspect the board for evidence of mishandling prior to applying power.

CAUTION
SENSITIVE ELECTRONIC DEVICES
USE ANTI-STATIC HANDLING PROCEDURES

2.2 CARD CAGE CONSIDERATIONS

Refer to the specifications for bus loading and power requirements. Be sure that the system power supplies are able to accommodate the additional requirements within the voltage tolerances specified.

Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature. Large and continuing fluctuations in ambient air temperature should be avoided. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air filtering.

2.3 BOARD CONFIGURATION

The board may be configured in a variety of ways for many different applications. Each possible jumper setting will be discussed in the following sections. The jumper locations are shown in Figure 2.1. Note that if you have a model containing the LED Expansion Board (-L suffix), it must be removed to change the digital input channel range jumpers (J9-J24). See Figure 2.2 for the LED Expansion Board assembly instructions.

2.3.1 Default Jumper Configuration

VMEbus INTERFACE CONFIGURATION

When a board is shipped from the factory, it is configured as follows:

- VMEbus Short I/O Address of 0000H.
- Set to respond to both Address Modifiers 29H and 2DH.
- Interrupt Level: none. Therefore, even if interrupts are enabled, no interrupts will be caused.

2.3.1.1 Digital Input Default Configuration

- 16 dedicated digital input points (numbered 0 through 15).
- All channels factory configured (via jumpers) for the 4-25V DC input range.
- Minimum input debounce selected.

2.3.1.2 Digital Output Default Configuration

- 16 dedicated digital output points (numbered 0 through 15).

2.4 VMEbus CONFIGURATION

2.4.1 Address Decode Jumper Configuration

The board interfaces with the VMEbus as a 1K block of address locations in the VMEbus Short I/O Address Space or Standard Address Space. J2 and J1 decode the fourteen most significant address lines A10 through A23 to provide segments of 1K address space. The configuration of the jumpers for different base address locations is shown below. "IN" means that the pins are shorted together with a shorting clip. "OUT" indicates that the clip has been removed. J2 decodes address lines A10 through A15 and J1 decodes Address lines A16 through A23. Therefore, when configured for the Short I/O Address space, only J2 needs to be configured.

Pins of J2						
BASE ADDR (HEX)	**A15 (11 & 12)**	**A14 (10 & 9)**	**A13 (8 & 7)**	**A12 (6 & 5)**	**A11 (4 & 3)**	**A10 (2 & 1)**
0000	OUT	OUT	OUT	OUT	OUT	OUT
0400	OUT	OUT	OUT	OUT	OUT	IN
0800	OUT	OUT	OUT	OUT	IN	OUT
0C00	OUT	OUT	OUT	OUT	IN	IN
1000	OUT	OUT	OUT	IN	OUT	OUT
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
EC00	IN	IN	IN	OUT	IN	IN
F000	IN	IN	IN	IN	OUT	OUT
F400	IN	IN	IN	IN	OUT	IN
F800	IN	IN	IN	IN	IN	OUT
FC00	IN	IN	IN	IN	IN	IN

Pins of J1								
BASE ADDR (HEX)	**A23 (15&16)**	**A22 (13&14)**	**A21 (11&12)**	**A20 (9&10)**	**A19 (7&8)**	**A18 (5&6)**	**A17 (3&4)**	**A16 (1&2)**
000000	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
010000	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN
020000	OUT	OUT	OUT	OUT	OUT	OUT	IN	OUT
030000	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
FC0000	IN	IN	IN	IN	IN	IN	OUT	OUT
FD0000	IN	IN	IN	IN	IN	IN	OUT	IN
FE0000	IN	IN	IN	IN	IN	IN	IN	OUT
FF0000	IN	IN	IN	IN	IN	IN	IN	IN

2.4.2 Address Modifier Jumper Configuration

The VMEbus Address Modifier jumpers (J3, J5, and J6) permit the board to respond to the various Address Modifier Codes.

Pins of J3,J5,J6				
J3 1&2	**J3 2&3**	**J5 1&2**	**J6 1&2**	**Address Modifier Code/Function**
OUT	IN	OUT	IN	2DH Only Short Supervisory Access
OUT	IN	IN	IN	2DH & 29H Short Supervisory Access and Short Non-privileged Access
IN	OUT	OUT	OUT	3DH Only Standard Supervisory Data Access
IN	OUT	IN	OUT	3DH & 39H Standard Supervisory Data Access
				and Standard Non-privileged Data Access

2.4.3 Interrupt Level Select Jumper Configuration

The board Interrupt Level is selected by configuring jumper J4 as follows:

Interrupt Level	J4 (5&6)	J4 (3&4)	J4 (1&2)
None	OUT	OUT	OUT
1	OUT	OUT	IN
2	OUT	IN	OUT
3	OUT	IN	IN
4	IN	OUT	OUT
5	IN	OUT	IN
6	IN	IN	OUT
7	IN	IN	IN

2.5 DIGITAL INPUT CONFIGURATION (9440-I & 9447-I)

Selectable input threshold voltages make the digital input points adaptable to almost any application. The inputs are designed for use with contact closures, switches, alarm trips, and power supply ON/OFF monitoring. Input points are optically isolated from each other and from the VMEbus. See Figure 2.3 for the simplified schematic of a digital input point.

Input channel debounce circuitry with selectable delay is also provided for each channel to eliminate glitches from the input signals. These glitches are frequently caused by contact bounce in mechanical relays and switches.

2.5.1 Digital Input Threshold Selection

Two input threshold voltages are selectable on a per channel basis by J9 to J24 to cover the input ranges from 4 to 55V DC, as shown in the following table:

Channel Range	J9-J24 1&2	J9-J24 2&3	Positive Threshold Voltage (Maximum)
4-25V DC	OUT	IN	4V DC
20-55V DC	IN	OUT	20V DC

2.5.2 Sensing Contact Closures and Switches

The input voltage should be within the range listed in the previous table. See Figure 2.4: Digital Input Point Configurations, for connections for different input types.

2.5.3 Debounce Delay Selection

If mechanical relay contacts (or switches) are used as inputs, it is strongly recommended that a debounce delay longer than the maximum expected bounce time be used. If the bounce time cannot be determined, then the maximum debounce delay should be selected.

The debounce delay time is jumper programmable (J7) on a global basis for all input channels (i.e. all input channels will have the same delay), as shown in the following table:

Debounce Delay Time (uS)	J7 1&2	J7 3&4	J7 5&6	J7 7&8
7 to 8	OUT	OUT	OUT	IN
336 to 384	OUT	OUT	IN	OUT
672 to 768	OUT	IN	OUT	OUT
1344 to1536	IN	OUT	OUT	OUT

NOTE: One of the debounce delay times must be selected. If none or more than one delay time is selected, the input signals will not pass through the debounce circuit.

2.6 DIGITAL OUTPUT CONFIGURATION (9440-I & 9443-I)

The Digital Outputs are designed to control valves, switch counters, mechanical relays, optical relays, indicator lamps, etc. Each digital output can be written to and then read back immediately for verification purposes, but for complete confidence in the output setting, the output should be fed back to an input point and the input point monitored. See Figure 2.5 for the simplified schematic of a digital output point. Outputs include reverse bias protection and a replaceable fuse (requires soldering). Output loads of up to 1 Amp DC and voltages up to 55V DC are supported.

2.6.1 Relay Coils and Other Inductive Loads

When driving relay coils or other inductive loads, diodes should be placed across each load to limit the voltage spike generated when an inductive load is switched off quickly. See Figure 2.6: Digital Output Point Configurations, for connections for different output types.

2.7 DIGITAL INPUT/OUTPUT INTERFACE TO TTL AND CMOS SIGNALS

Logic level inputs can be interfaced to the board by the use of common logic elements such as the 74LS05 (or 74HC05) open collector (or drain) inverter gates. See Figure 2.7: Interface to TTL and CMOS Signals, for connection information. Applying a logic "1" to the input of the inverter gate sinks the current required to turn the optically-coupled logic gate on (using the lowest input voltage range) and yields a logic "1" for the corresponding input channel register bit position.

Logic level outputs are easily interfaced by the use of 74LS04 (or 74HC04) inverter gates. Programming a logic "1" in the corresponding output channel register bit position turns on the output SSR which pulls the input to the inverter gate low. This yields a logic "1" at the output of the inverter gate.

2.8 CONNECTORS

2.8.1 Digital Input Connector

Digital inputs are connected to the 944x via connector P4 (lower connector as viewed from the front). Table 2.1 defines the assignment. These connections are easily accommodated through the use of Acromag termination panels and flat cable assemblies or through the use of a user defined termination panel.

P4: Panduit No. 100-532-053; Series 100, Type B Male Connectors, rows A & B equipped, even pins only (32 pins total).

Table 2.1: P4 CONNECTOR

Pin Number	Mnemonic	Pin Number	Mnemonic
32A	CH0+	32B	CH0-
30A	CH1+	30B	CH1-
28A	CH2+	28B	CH2-
26A	CH3+	26B	CH3-
24A	CH4+	24B	CH4-
22A	CH5+	22B	CH5-
20A	CH6+	20B	CH6-
18A	CH7+	18B	CH7-
16A	CH8+	16B	CH8-
14A	CH9+	14B	CH9-
12A	CH10+	12B	CH10-
10A	CH11+	10B	CH11-
8A	CH12+	8B	CH12-
6A	CH13+	6B	CH13-
4A	CH14+	4B	CH14-
2A	CH15+	2B	CH15-

2.8.2 Digital Output Connector

Digital outputs are connected to the 944x via connector P3 (upper connector as viewed from the front). Table 2.2 defines the assignment. These connections are easily accommodated through the use of Acromag termination panels and flat cable assemblies or through the use of a user defined termination panel.

P3: Panduit No. 100-532-053; Series 100, Type B Male Connectors, rows A & B equipped, even pins only (32 pins total).

Table 2.2: P3 CONNECTOR

Pin Number	Mnemonic	Pin Number	Mnemonic
32A	CH0+	32B	CH0-
30A	CH1+	30B	CH1-
28A	CH2+	28B	CH2-
26A	CH3+	26B	CH3-
24A	CH4+	24B	CH4-
22A	CH5+	22B	CH5-
20A	CH6+	20B	CH6-
18A	CH7+	18B	CH7-
16A	CH8+	16B	CH8-
14A	CH9+	14B	CH9-
12A	CH10+	12B	CH10-
10A	CH11+	10B	CH11-
8A	CH12+	8B	CH12-
6A	CH13+	6B	CH13-
4A	CH14+	4B	CH14-
2A	CH15+	2B	CH15-

2.8.3 VMEbus Connections

Table 2.3 indicates pin assignments for the VMEbus signals at the P1 connector. The P1 connector is the upper connector on the 944x board as viewed from the front. The connector consists of 32 rows of three pins labeled A, B, and C. Pin A1 is located at the upper left hand corner of the connector.

TABLE 2.3: P1 BUS CONNECTIONS

PIN	NUMBER MNEMONIC	PIN	NUMBER MNEMONIC	PIN	NUMBER MNEMONIC
1A	D00	1B	BBSY*	1C	D08
2A	D01	2B	BCLR *	2C	D09
3A	D02	3B	ACFAIL*	3C	D10
4A	D03	4B	BG0IN*	4C	D11
5A	D04	5B	BG0OUT*	5C	D12
6A	D05	6B	BG1IN*	6C	D13
7A	D06	7B	BG1OUT*	7C	D14
8A	D07	8B	BG2IN*	8C	D15
9A	GND	9B	BG2OUT*	9C	GND
10A	SYSCLK	10B	BG3IN*	10C	SYSFAIL*
11A	GND	11B	BG3OUT*	11C	BERR*
12A	DS1*	12B	BR0*	12C	SYSRESET*
13A	DS0*	13B	BR1*	13C	LWORD*
14A	WRITE*	14B	BR2*	14C	AM5
15A	GND	15B	BR3*	15C	A23
16A	DTACK*	16B	AM0	16C	A22
17A	GND	17B	AM1	17C	A21
18A	AS*	18B	AM2	18C	A20
19A	GND	19B	AM3	19C	A19
20A	IACK*	20B	GND	20C	A18
21A	IACKIN*	21B	SERCLK	21C	A17
22A	IACKOUT*	22B	SERDAT*	22C	A16
23A	AM4	23B	GND	23C	A15
24A	A07	24B	IRQ7*	24C	A14
25A	A06	25B	IRQ6*	25C	A13
26A	A05	26B	IRQ5*	26C	A12
27A	A04	27B	IRQ4*	27C	A11
28A	A03	28B	IRQ3*	28C	A10
29A	A02	29B	IRQ2*	29C	A09
30A	A01	30B	IRQ1*	30C	A08
31A	-12V	31B	+5V STDBY	31C	+12V
32A	+5V	32B	+5V	32C	+5V

* Indicates that the signal is active low.

Refer to the VMEbus specification for additional information on the VMEbus signals.

2.9 POWER-UP TIMING AND LOADING

The 944x board uses a Logic Cell Array to handle the bus interface and control logic timing. Upon power-up, the Logic Cell Array automatically clocks in configuration vectors from a local PROM to initialize the logic circuitry for normal operation. This time is measured as the first 145 mS (typical) after the +5 Volt supply raises to +2.5 Volts at power-up. If a data transfer is attempted during this time, it will simply be ignored and the board will not respond. This should not be a problem because the VME specification requires that the bus master drive the system reset for the first 200 mS after power-up, thus inhibiting any data transfers from taking place.

Digital input and output channels are reset to the OFF state following a power-up sequence. External input signals above threshold levels can then drive inputs ON. Likewise, writing to the digital output registers can program outputs ON.

2.10 DATA TRANSFER TIMING

Data transfer time is measured from the falling edge of DSx* to the falling edge of DTACK* during a normal data transfer cycle.

REGISTER	DATA TRANSFER TIME
All Registers	580nS, typical

2.11 FIELD GROUNDING CONSIDERATIONS

The board is designed to isolate every input and output channel from each other as well as from the VMEbus. This is intended to protect each channel and the VMEbus from voltage spikes and transients such as those caused by ground currents and "pick-up". The isolation provides the ability to earth ground the field wiring without the concern of ground currents damaging the card cage electronics.

3.0 PROGRAMMING INFORMATION

This chapter provides the specific information necessary to operate the Isolated Digital I/O Board.

3.1 MEMORY MAP

The board is addressable on 1K byte boundaries in the Short I/O Address Space or Standard Address Space. All Acromag VMEbus non-intelligent slaves have a standard interface configuration which consists of a 32 byte board ID PROM and a Board Status register. The rest of the 1K byte address space contains registers or memory specific to the function of the board. The memory map is shown in Figure 3.1 (Addresses in Hex).

Figure 3.1: Board Memory Map

Address Base + (HEX)	D15 Even D8	D7 Odd D0	Address Base + (HEX)
00 ↓ 3E	Undefined	R - Board ID PROM	01 ↓ 3F
40 ↓ 7E	Undefined	Undefined	41 ↓ 7F
80	Undefined	R/W - Board Status	81
82 ↓ 9E	Undefined	Undefined	83 ↓ 9F
A0	Undefined	R/W - Int. Vector CH0	A1
A2	"	R/W - Int. Vector CH1	A3
A4	"	R/W - Int. Vector CH2	A5
A6	Undefined	R/W - Int. Vector CH3	A7
A8	"	R/W - Int. Vector CH4	A9
AA	"	R/W - Int. Vector CH5	AB
AC	"	R/W - Int. Vector CH6	AD
AE	"	R/W - Int. Vector CH7	AF
B0 ↓ BE	Undefined	Undefined	B1 ↓ BF
C0	Undefined	R/W - Digital Input Channel Interrupt Status Register CH7 CH0	C1
C2	Undefined	R/W - Digital Input Channel Interrupt Enable Register CH7 CH0	C3
C4	Undefined	R/W - Digital Input Channel Interrupt Polarity Register CH7 CH0	C5
C6	Undefined	R/W - Digital Input Channel Interrupt Type Select Register CH7 CH0	C7
C8	Undefined	R/W - Digital Input Channel Int. Pattern Enable Register CH7 CH0	C9
CA	R - Digital Input Channel Data Register CH15 CH0		CB
CC	R/W - Digital Output Channel Data Register CH15 CH0		CD
CE ↓ 3EF	Undefined	Undefined	CF ↓ 3FF

3.1.1 Board Identification PROM - (read only) - 01H through 3FH (odd)

The board contains an identification section. This section of data describes the board model number and the manufacturer. The identification section starts at the board's base address plus 1 and is 32 bytes in length. Bytes are addressed using only the odd addresses between 1 and 63. The PROM contents are shown in Figure 3.2 for an AVME9440-I-L (each model has a unique PROM).

Figure 3.2: AVME9440-I-L Board Identification PROM

Offset From Board Base Address	**Value**		**Descriptions**
	ASCII Character	**Numeric**	
01H	V	56H	All boards have "VMEID"
03H	M	4DH	
05H	E	45H	
07H	I	49H	
09H	D	44H	
0BH	A	41H	Manufacturer's I.D., "ACR" for
0DH	C	43H	Acromag
0FH	R	52H	
11H	9	39H	Board Model Number (6 characters
13H	4	34H	and 1 trailing "blank")
15H	4	34H	
17H	0	30H	(Each model has a unique number)
19H	I	49H	
1BH	L	4CH	
1DH		20H	
1FH	1	31H	Number of KILOBYTES of address space used.
21H		20H	
23H	Undefined		Reserved
25H	"		"
27H	"		"
29H	"		"
2BH	"		"
2DH	"		"
2FH	"		"
31H	"		"
33H	"		"
35H	"		"
37H	"		"
39H	"		"
3BH	"		"
3DH	"		"
3FH	Undefined		Reserved

3.1.2 Board Status Register - (read/write) - 81H

The Board Status Register reflects and controls functions globally on the board.

MSB 7	6	5	4	3	2	1	LSB 0
<------ Reserved ------>			Software Reset	Global Int. Enable	Global Int. Pending	Green LED	Red LED

Where:

Bits 7,6,5: Reserved for future use - equal "0" if read.

Bit 4: Software Reset (W) - writing a "1" to this bit causes a software reset. Writing "0" or reading the bit has no effect. The effect of a software reset on the various registers is described in the description of each register.

Reset Condition: Set to "0".

Bit 3: Global Interrupt Enable (R/W) - writing a "1" to this bit enables interrupts to be serviced, provided the interrupt level (IRQx*) is selected. A "0" disables servicing interrupts.

Reset Condition: Set to "0", interrupts disabled.

Bit 2: Global Interrupt Pending (R) - this bit will be a "1" when there is an interrupt pending. This bit will be "0" when there is no interrupt pending. Polling this bit will reflect the board's pending interrupt status, even if the Global Interrupt Enable bit is set to "0".

Reset condition: Set to "0".

Bit 1: Green LED (R/W) - when written, this bit will control the state of the green LED on the front panel. A "1" will turn it on, a "0" will turn it off. Reading it will reflect its current state.

Reset Condition: Set to "0", green LED off.

Bit 0: Red LED (R/W) - when written, this bit will control the state of the red LED on the front panel and the state of the VMEbus SYSFAIL* signal. A "1" will turn the LED off and set SYSFAIL* high, a "0" will turn the LED on and set SYSFAIL* low. Reading it will reflect its current state. (See Section 5.2 for additional information on using SYSFAIL*.)

Reset Condition: Set to "0", red LED lit, and SYSFAIL* is set low.

3.1.2.1 Status Bits Usage

The status register bits 1 and 0 along with the green and red LEDs provide the user with a means of keeping track of a board's functionality in the system. Since there is no intelligence on the board, the host computer controls these bits. The following paragraphs and summary table describe possible uses of the bits in the status register and the LEDs on the front panel.

On power-up the bits in the status register read low, with the green LED off, the red LED lit, and SYSFAIL* low. This indicates that the board has failed or that it has not been tested yet.

If the status register bit 1 reads low and Bit 0 reads high, the LEDs will both be off and SYSFAIL* high. This indicates an inactive board.

If the status register bit 1 reads high and Bit 0 reads low, the LEDs will both be lit and SYSFAIL* low. This indicates the board is undergoing a diagnostic checkout.

If the status register bits 1 and 0 read high, the green LED will be lit with the red LED off and SYSFAIL* high. This indicates the board is fully functional.

Status Bits - Possible Usage

Bit 0 (Red LED)	Bit 1 (Green LED)	SYSFAIL*	Description
0, (on)	0, (off)	Low	Failed or reset condition
1, (off)	0, (off)	High	Inactive board
0, (on)	1, (on)	Low	Diagnostics are running
1, (off)	1, (on)	High	Normal operation

3.1.3 Interrupt Vector Registers - (read/write) - A1H to AFH (Odd addresses)

The interrupt vector registers maintain the 8 bit interrupt vector numbers for each of the 8 digital input channel interrupt lines. Note that interrupts can only be generated for digital input channels 0-7. The appropriate vector is provided to the VMEbus Interrupt Handler when an interrupt is being serviced. This allows each digital input channel interrupt to be serviced by its own software handler. If desired, a single handler can be used by making all of the vectors the same. In this case, the handler will have to determine the interrupting channel by examining the interrupt status register.

The register content is undefined upon reset.

3.1.4 Digital Input Channel Interrupt Status Register (read/write) - C1H

The digital input channel interrupt status register reflects the status of the 8 input channels (ch. 0-7). A "1" in a bit position indicates an interrupt is pending for the corresponding channel. Each bit is derived from the logical AND of its associated interrupt input and enable bits. Hence, an input channel that does not have interrupts enabled cannot have its interrupt pending bit set to a "1".

An individual channel's interrupt can be cleared by writing a "1" to its bit position in the interrupt status register. However, if the condition which caused the interrupt remains or reappears, a new interrupt will be generated. To permanently disable a channel's interrupt, the corresponding bit in the channel interrupt enable register must be cleared, followed by writing a "1" to the channel's bit position in the channel interrupt status register (to clear the interrupt). This is known as the "Release On Register Access" (RORA) method as defined in the VME system architecture.

Bit 7 of this register has a dual purpose. In addition to indicating an interrupt for channel 7, it is also used to indicate an input channel bit pattern match (see the digital input channel interrupt pattern enable register).

MSB 7	6	5	4	3	2	1	LSB 0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

All interrupts are cleared following a reset.

NOTE: Interrupts are prioritized via hardware within the card. Channel 7 is the highest priority and channel 0 is the lowest. If multiple input channel interrupts become pending simultaneously, the vector corresponding to the

highest numbered channel will be delivered first. After the highest channel's interrupt is serviced and cleared, an additional interrupt will be generated for the next highest priority interrupt (pending) channel.

NOTE: Input channel bandwidth should be limited to reduce the possibility of missing channel interrupts. For a specific input channel this could happen if multiple changes occur before the channel's interrupt is serviced.

3.1.5 Digital Input Channel Interrupt Enable Register (read/write) - C3H

The digital input channel interrupt enable register provides a mask bit for each of the 8 input channels (ch. 0-7). A "0" in a bit position will prevent the corresponding input channel from causing an external interrupt. A "1" will allow the input channel to cause an interrupt (providing that the global interrupt enable bit is set).

MSB 7	6	5	4	3	2	1	LSB 0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

All input channel interrupts are masked ("0") following a reset.

3.1.6 Digital Input Channel Interrupt Polarity Register (read/write) - C5H

The digital input channel interrupt polarity register determines the level that will cause a channel interrupt for each of the 8 input channels (ch. 0-7). A "0" in a bit position means an interrupt will occur when the input channel is below threshold (i.e. a "0" in the digital input channel data register). A "1" in a bit position means an interrupt will occur when the input channel is above threshold (i.e. a "1" in the digital input channel data register).

Note that interrupts will not occur unless they are enabled. The interrupt polarity register will have no effect if Change Of State (COS) interrupts are selected (see the digital input channel interrupt type select register).

MSB 7	6	5	4	3	2	1	LSB 0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

All bits are set to "0" following a reset which means that the inputs will cause interrupts when they are below threshold.

3.1.7 Digital Input Channel Interrupt Type Select Register (read/write) - C7H

The digital input channel interrupt type select register determines the type of input channel behavior that will cause a channel interrupt for each of the 8 input channels (ch. 0-7). A "0" in a bit position means an interrupt will be generated when the input channel level specified by the digital input channel interrupt polarity register occurs. A "1" in a bit position means an interrupt will occur when a Change Of State (COS) occurs at the input channel (either low to high, or high to low).

Note that interrupts will not occur unless they are enabled.

MSB 7	6	5	4	3	2	1	LSB 0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

All bits are set to "0" following a reset which means that the inputs will cause interrupts for the input channel levels specified by the digital input channel interrupt polarity register.

3.1.8 Digital Input Channel Interrupt Pattern Enable Reg. (read/write) - C9H

The digital input channel interrupt pattern enable register provides a mask bit for each of the 8 input channels (ch. 0-7). A "0" in a bit position will prevent the corresponding input channel from being part of a pattern of channels (bits) which can cause an interrupt. A "1" will allow the input channel to be a component of a pattern which can cause an interrupt. Note that an interrupt will only be generated if all enabled channels (at least 1 and up to 8 channels) forming the pattern meet the level requirements specified in the digital input channel interrupt polarity register (providing that the global interrupt enable bit is set). Note that when pattern interrupts are desired, the digital input channel interrupt type select register bits must be set to "0" (interrupt on input level, not on change of state).

Note also that the interrupt generated will result in setting the status bit in the digital input channel interrupt status register which corresponds to channel 7 (i.e. the highest priority channel).

MSB 7	6	5	4	3	2	1	LSB 0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

All input channel pattern enable bits are masked ("0") following a reset.

3.1.9 Digital Input Channel Data Register (read) - CAH & CBH

The digital input channel data register represents the actual state of the 16 digital input channels at the time the register is read (note that the debounce circuit will insert a delay dependent on the degree of debounce selected). A "0" means that the signal across the board's input channel connector is below threshold. A "1" means that the signal is above threshold. Note that the threshold voltage (i.e. range) is selectable.

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

3.1.10 Digital Output Channel Data Register (read/write) - CCH & CDH

When the digital output channel data register is written to, the value written is represented on the output channels. A "0" means that the corresponding output channel's Solid State Relay (SSR) is open (off). A "1" means that the SSR is closed (on).

Each digital output can be written to and then read back immediately for verification purposes, but for complete confidence in the output setting, the output should be fed back to an input point and the input point monitored.

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

All bits are set to "0" following a reset which means that the output SSR is OFF.

3.2 GENERAL PROGRAMMING CONSIDERATIONS

3.2.1 Board Diagnostics

The board is a non-intelligent slave and does not perform self diagnostics. It does, however, provide a standard interface architecture which includes a Board Status Register useful in system diagnostics.

Status bits, control of front panel LEDs, and control of the SYSFAIL* signal are provided through the Board Status Register. Bits 0 and 1 may be used as follows:

Board Status Register Bit 1	Bit 0	LEDs Green	Red	SYSFAIL* Signal	Condition
0	0	Off	On	On	Board failed test or has not been tested.
1	0	On	On	On	Board is being tested.
1	1	On	Off	Off	Board has passed test.
0	1	Off	Off	Off	Board is inactive.

At power up, the system diagnostic software can test each non-intelligent Slave, sequencing the status bits to indicate "undergoing test" and then to "passed" or "failed".

After testing each board, the system software records which boards have failed and sets their status to indicate "inactive". By setting the board's status to inactive, the SYSFAIL* signal is released and may then be useful for an on-line indication of failure by other boards.

Alternatively, the system software could simply set the bits and therefore front panel LEDs, to "passed test" as a visual indication that the presence of the board is recognized.

3.3 GENERATING INTERRUPTS

Digital input channels 0-7 can cause interrupts to be generated for a wide variety of conditions. These include interrupts for:

- Change Of State (COS) of selected input channels.
- Input level (polarity) match of selected input channels.
- Input pattern match of the levels of multiple input channels.

The interrupt level (IRQx*) associated with the card is programmable via a jumper on the board. The interrupt release mechanism is the Release On Register Access (RORA) type. This means that the interrupter will release the interrupt request line (IRQx*) after the interrupt has been cleared by writing a "1" to the appropriate bit position in the input channel interrupt status register.

The user has the option of having a single interrupt handler for the entire board or having each channel serviced by a separate software handler. This is determined by what is written into the interrupt vector registers. There is a unique register for each digital input channel (0-7). However, if the user programs the same vector into all of the vector registers, then the board will have a single interrupt handler.

The digital input channels are prioritized with respect to their interrupts. Channel 7 is the highest priority and channel 0 is the lowest. If multiple input channel interrupts become pending simultaneously, the vector corresponding to the highest numbered channel will be delivered first. After the highest channel's interrupt is serviced and cleared, an additional interrupt will be generated for the next highest priority interrupt (pending) channel. If an input channel pattern match is generated, the interrupt will appear in the channel 7 (i.e. the highest priority) position in the interrupt status register.

Input channel bandwidth should be limited to reduce the possibility of missing channel interrupts. For a specific input channel this could happen if multiple changes occur before the channel's interrupt is serviced.

When configuring and enabling interrupts the response time of the input channels should be considered. The digital input channel response time is the sum of the response times of the optically coupled logic gate (1uS. typical, 7uS. maximum), the debounce circuit (7uS. to 1.54mS., user selected), and the interrupt logic circuit (1uS. to 192uS., follows debounce selection) as illustrated in Figure 3.3. The total response time must pass before an input channel stimulus (matching an interrupt condition) will be recognized.

Likewise, if an input channel stimulus is programmed to the polarity (level) which should not cause an interrupt, the board user should wait for the response time to pass before enabling interrupts from the channel (see Figure 3.3). To do otherwise will capture an "old" signal which has not completely propagated through the circuit and cause an unwanted interrupt.

3.3.1 Interrupt Example For Change Of State (COS)

1. Set interrupt level (IRQx*) associated with the board via jumper (J4).
2. Clear the global interrupt enable bit in the Board Status Register by writing a "0" to bit 3.
3. Write vectors into the Digital Input Channel Interrupt Vector Registers.
4. Select COS interrupts for channels by writing "1" to each channel's associated bit in the Digital Input Channel Interrupt Type Select Register.
5. Disable input pattern detection interrupts by writing "0" to each channel's associated bit in the Digital Input Channel Interrupt Pattern Enable Register.
6. Enable individual input channel interrupts by writing "1" to each channel's associated bit in the Digital Input Channel Interrupt Enable Register.
7. Clear pending interrupt inputs by writing "1" to each channel's associated bit in the Digital Input Channel Interrupt Status Register.
8. Enable interrupts from the board by writing a "1" to bit 3 (the global interrupt enable bit) in the Board Status Register.

Interrupts may now occur from the board.

3.3.2 Interrupt Example For Input Level (Polarity) Match

1. Set interrupt level (IRQx*) associated with the board via jumper (J4).
2. Clear the global interrupt enable bit in the Board Status Register by writing a "0" to bit 3.
3. Write vectors into the Digital Input Channel Interrupt Vector Registers.
4. Select polarity (level) interrupts for channels by writing "0" to each channel's associated bit in the Digital Input Channel Interrupt Type Select Register.

5. Select the desired polarity (level) for input channel interrupts by writing "0" or "1" to each channel's associated bit in the Digital Input Channel Interrupt Polarity Register.
6. Disable input pattern detection interrupts by writing "0" to each channel's associated bit in the Digital Input Channel Interrupt Pattern Enable Register.
7. Enable individual input channel interrupts by writing "1" to each channel's associated bit in the Digital Input Channel Interrupt Enable Register.
8. Clear pending interrupt inputs by writing "1" to each channel's associated bit in the Digital Input Channel Interrupt Status Register.
9. Enable interrupts from the board by writing a "1" to bit 3 (the global interrupt enable bit) in the Board Status Register.

Interrupts may now occur from the board.

3.3.3 Interrupt Example For Input Pattern Match (Of Multiple Channel Levels)

1. Set interrupt level (IRQx*) associated with the board via jumper (J4).
2. Clear the global interrupt enable bit in the Board Status Register by writing a "0" to bit 3.
3. Write vector into the Digital Input Channel Interrupt Vector Register associated with channel 7.
4. Select polarity (level) interrupts for channels by writing "0" to each channel's associated bit in the Digital Input Channel Interrupt Type Select Register.
5. Select the desired polarity (level) for input channel interrupts by writing "0" or "1" to each channel's associated bit in the Digital Input Channel Interrupt Polarity Register.
6. Disable individual input channel interrupts by writing "0" to each channel's associated bit in the Digital Input Channel Interrupt Enable Register.
7. Enable input pattern detection interrupts by writing "1" to each channel's associated bit in the Digital Input Channel Interrupt Pattern Enable Register.
8. Clear pending interrupt inputs by writing "1" to each channel's associated bit in the Digital Input Channel Interrupt Status Register.
9. Enable interrupts from the board by writing a "1" to bit 3 (the global interrupt enable bit) in the Board Status Register.

Interrupts may now occur from the board.

3.3.4 Sequence of Events For an Interrupt

1. The AVME944x (interrupter) board makes an interrupt request (asserts IRQx*).
2. The host (interrupt handler) asserts IACK* and the level of the interrupt it is seeking on A01-A03.
3. When the asserted IACKIN* signal (daisy chained) is passed to the 944x, the board will put the appropriate interrupt vector on the bus (D00-D07), if the level of the interrupt matches that sought by the host. Note that IRQx* remains asserted.
4. The host uses the vector to point at which interrupt handler to execute and begins its execution.
5. Example of Generic Interrupt Handler Actions:
   A. Disable the interrupting channel(s) by writing a "0" to the appropriate bits in the interrupt enable register.
   B. Clear the interrupting channel(s) by writing a "1" to the appropriate bits in the interrupt status register.
   C. Enable the interrupting channel(s) by writing a "1" to the appropriate bits in the interrupt enable register.
6. If the input stimulus has been removed and no other channels have interrupts pending, the interrupt cycle is completed (i.e. the board negates its interrupt request, IRQx*).

A. If the input stimulus remains, a new interrupt request will immediately follow. If the stimulus cannot be removed, then the channel should be disabled or reconfigured (e.g. for the opposite polarity).
B. If other channels have interrupts pending, then the interrupt request (IRQx*) will remain asserted. This will start a new interrupt cycle.

4.0 THEORY OF OPERATION

This chapter describes the circuitry that is used on the board. A block diagram is shown in Figure 4.1. Parts lists are in chapter 5, and the schematic & part location drawings are near the end of this manual.

4.1 VMEbus INTERFACE

The VMEbus interface is composed of three functional circuit areas.

- Data buffers (U54, U55)
- Interrupter (U51, U56, U57, U62, U63)
- Address decode and bus control logic (U51, U58, U59, U60)

4.1.1 VMEbus Control Logic

The Data Transfer Acknowledge (DTACK*) signal is generated by the logic/timing circuitry (U51, U58) on the board for handshaking with the bus master during data transfer cycles. The DTACK* signal will be asserted after the card address has been properly decoded and either of the data strobes (DS1*, DS0*) is asserted. The amount of delay before DTACK* is asserted is controlled by circuitry within U51 which uses the SYSCLK (16MHz.) provided on the VMEbus to derive a fixed time delay.

The AVME944x does not use (assert) the VME BERR* signal (as permitted in the VMEbus specification). If the bus master improperly addresses the board, it will not get a response, however the VMEbus Bus Timer located in the System Controller will time-out and cause an end to the cycle.

4.1.2 VME Interrupter

The interrupt level (IRQx*) associated with the card is programmable via a jumper on the board. The card will return an 8-bit interrupt vector during the interrupt acknowledge cycle. Each interrupting channel can have its own interrupt vector. The interrupt release mechanism is the Release On Register Access (RORA) type. This means that an interrupter will release the interrupt request line (IRQx*) after the interrupt has been cleared by writing a "1" to the appropriate bit position in the input channel interrupt status register.

Interrupts can be generated by any of 8 digital inputs (channels 0-7). Interrupt on selected input channel COS or polarity (level) match can be selected. Alternatively, interrupts on a pattern match of selected input channel polarities (levels) can be programmed. Interrupts occur on a first come first served basis, unless they occur at the same time. If two or more interrupts occur at the same time, then channel 7 has the highest priority (channel 0 has the lowest). If an input channel pattern match is generated, the interrupt will appear in the channel 7 (highest priority) position.

Input channel bandwidth should be limited to reduce the possibility of missing channel interrupts. For a specific input channel this could happen if multiple changes occur before the channel's interrupt is serviced.

When an input channel interrupt condition is satisfied, the interrupter logic will assert the pre-programmed interrupt request level (IRQ7* - IRQ1*) and then monitor the Interrupt Acknowledge Input (IACKIN*) signal. When IACKIN* is asserted the logic compares the VMEbus address lines (A1 - A3) to the pre-programmed board interrupt level. If the lines are not equal, it will pass the signal along by asserting IACKOUT*. If the lines are equal, it will then drive the data bus D08 (O) with the vector associated with the interrupting channel and assert the DTACK* signal.

The interrupt vector registers are contained in U62. Both U51 and U63 control the addressing of the vector registers. The board status register is in U51. All other interrupt configuration and status registers, as well as input channel interrupt logic and priority encoding, are in U63. U56 performs the board interrupt level decoding, and U57 checks for a match of the bus interrupt level to the board interrupt level. The IACKIN* signal is monitored by U51, which controls both IACKOUT* and DTACK* signals.

4.2 REGISTER LOCATION SUMMARY

Local memory locations are implemented in various data registers on board. The registers are located in the following devices:

- Board Identification PROM (U61)
- Board Status Register (U51)
- Interrupt Vector Registers (U62)
- Digital Input Channel Interrupt Status Register (U63)
- Digital Input Channel Interrupt Enable Register (U63)
- Digital Input Channel Interrupt Polarity Register (U63)
- Digital Input Channel Interrupt Pattern Enable Register (U63)
- Digital Input Channel Interrupt Type Select Register (U63)
- Digital Input Channel Data Register (U63)
- Digital Output Channel Data Register (U1, U2)

4.3 ISOLATION BARRIER

Optical isolation is used to isolate all digital input and output channels from each other (channel to channel) and from the logic and VMEbus circuits.

4.4 DIGITAL INPUT SECTION (9440-I & 9447-I)

There are 16 digital input channels available on the board. A jumper (J9-J24) is used to select the DC input voltage range for each channel, and an optically-coupled logic gate (U19-U34) detects the input state.

Input channel debounce circuitry is also provided (U64) for each channel to eliminate glitches from the input signals. These glitches are frequently caused by contact bounce in mechanical relays and switches. Eliminating these glitches is desirable to prevent erroneous channel data and spurious interrupts. The debounce delay time is jumper programmable (J7) on a global basis for all input channels (i.e. all input channels will have the same delay).

4.5 DIGITAL OUTPUT SECTION (9440-I & 9443-I)

There are 16 digital output channels available on the board. Optically coupled, Solid State Relays (SSRs) provide the single pole, single throw normally open (SPST-NO), relay function (U3-U18). The SSRs cover the wide DC output voltage range without requiring range jumpers. Digital outputs may be read back (prior to the optical isolation) for verification purposes. Reverse polarity protection and a replaceable fuse (soldering required) are also provided for each channel.

5.0 SERVICE AND REPAIR INFORMATION

This chapter provides instructions on how to obtain service and repair assistance, service procedures, and component parts lists.

5.1 SERVICE AND REPAIR ASSISTANCE

It is highly recommended that a non-functioning board be returned to Acromag for repair. Acromag uses tested and burned-in parts, and in some cases, parts that have been selected for characteristics beyond that specified by the manufacturer. Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

5.2 PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Chapter 2, Preparation For Use, have been followed. The procedures are necessary since the board has jumpers that must be properly configured.

CAUTION
POWER MUST BE OFF BEFORE REMOVING OR INSERTING BOARDS

Note: It has been observed that on occasion, a "boot" program for a disk operating system will "hang" waiting for the VMEbus SYSFAIL* signal to be released by an intelligent disk controller board. Acromag's non-intelligent slave boards assert the SYSFAIL* signal as described in the VMEbus Specification Rev. C.1 and therefore, the disk operating system will remain "hung". The best solution to this problem is to correct the boot program so that it is no longer dependent upon the SYSFAIL* signal. When this solution is not practical, it is possible to disconnect the SYSFAIL* from the circuitry on the Acromag board by cutting a PC board foil near the P1 connector on the solder side. Caution should be exercised so as not to cut any other foils nor damage the board in any other way. Call Acromag's Applications Engineering Department for assistance.

5.3 PARTS LISTS

Parts Lists are provided as an aid to the user in troubleshooting the Board (also reference the schematic and part location drawings. Tables 5.1A to 5.1D list the parts installed on the main board for the various models; similarly Tables 5.2A to 5.2C list parts for the LED expansion board. Replacement parts and repair services are available from Acromag.

Changes are sometimes made to improve the product, to facilitate delivery, or to control cost. It is therefore important to include the Component Reference Number, the Acromag Part Number, the Board Model Number, and the Board Serial Number when providing information to order parts.

TABLE 5.1A: PARTS LIST FOR MODEL AVME944x-I)
(MAIN BOARD - PARTS COMMON TO ALL MODELS)

COMPONENT REFERENCE NUMBER	ACROMAG PART NUMBER	DESCRIPTION
U51	1033-578	IC XC3030-70PC84C
U52	5024-535	Programmed part
U53	1033-670	IC 74LS174N
U54,55	1033-627	IC 74LS645-1ND
U56	1033-048	IC 7445N
U57	1033-719	IC 74LS136N3
U58	1033-623	IC 74F38N
U59,60	1033-626	IC AM25LS2521PCB
R21	1100-268	RES NETWORK 9 4700 OHM
R22	1000-825	RES FILM 5% .25W 330 OHM
R23	1000-822	RES FILM 5% .25W 180 OHM
R24,25	1100-494	RES NETWORK 7 1K
R26,27	1000-839	RES FILM 5PC .25W 4.7K
C19,20,24,25,27-29	1002-530	CAP MONO 0.1UF 100V Z5U
C21	1002-606	CAP 16 PIN DIP 0.03UF
C22,23	1002-608	CAP 20 PIN DIP 0.03UF
C26	1002-605	CAP 14 PIN DIP 0.02UF
C30	1002-314	CAP TAN 150UF 15V
D17	1001-197	LED BILEVEL RED/GRN
D18	1001-113	DIODE IN914B
X1	1004-606	CHIP CARRIER, 84 PIN
P1	1004-505	CONN. EDGE 96 PIN MALE RT
P5-8	1004-626	HEADER 9 POST SHORT
J1	1004-379	HEADER 16 POST 2 ROW
J2	1004-383	POST 2 ROW 12 POSITION
J3	1004-333	HEADER 3 PIN POST
J4	1004-374	HEADER 6 POST 2 ROW
J5,6	1004-410	POSTS 1 ROW 2 POS
ITEM	1004-332	CLIP BUCK SHORTING

TABLE 5.1B: PARTS LIST FOR MODEL AVME9443-I)
(MAIN BOARD - PARTS UNIQUE TO THIS MODEL)

COMPONENT REFERENCE NUMBER	ACROMAG PART NUMBER	DESCRIPTION
U1,2	1033-777	IC SN74ALS996NT
U3-18	1033-614	IC HSSR-8060
U61	5024-527(-528)	Programmed part (-L option)
R1,2	1100-635	RES NET 2% 9-COM 270 OHM
R28,29	1100-490	RES NET 9 1K
C1-2	1002-530	CAP MONO 0.1UF 100V Z5U
D1-16	1001-176	DIODE ZENER 1N4761A
P3	1004-687	CONN. 32 POS RA PC MOUNT
F1-16	1030-496	FUSE PICO 2 AMP
J25	2002-305	JUMPER TEFLON 0.30

TABLE 5.1C: PARTS LIST FOR MODEL AVME9440-I)
(MAIN BOARD - PARTS UNIQUE TO THIS MODEL)

COMPONENT REFERENCE NUMBER	ACROMAG PART NUMBER	DESCRIPTION
U1,2	1033-777	IC SN74ALS996NT-3
U3-18	1033-614	IC HSSR-8060
U19-34	1033-616	IC H11L1
U61	5024-525(-526)	Programmed part (-L option)
U62	1033-417	TMM2015AP-15
U63	1033-578	IC XC3030-70PC84C
U64	1033-715	IC XC2018-50PC84C
U65	5024-536	Programmed part
R1,2,19,20	1100-635	RES NET 2% 9-COM 270 OHM
R3-18	1100-775	RES NET 2% 9-COM HIP 10K
R28,29	1100-490	RES NET 9 1K
R30	1000-836	RES FILM 5% .25W 2.7K OHM
C1,2,7,8,13,14,31-34	1002-530	CAP MONO 0.1UF 100V Z5U
D1-16	1001-176	DIODE ZENER 1N4761A
D19	1001-113	DIODE 1N914B
X2,3	1004-606	CHIP CARRIER, 84 PIN
P3,4	1004-687	CONN. 32 POS RA PC MOUNT
P9	1004-410	POSTS 1 ROW 2 POS
J7	1004-377	HEADER 8 POST 2 ROW
J9-24	1004-621	HEADER 3 POST SHORT
F1-16	1030-496	FUSE PICO 2 AMP

TABLE 5.1D: PARTS LIST FOR MODEL AVME9447-I)
(MAIN BOARD - PARTS UNIQUE TO THIS MODEL)

COMPONENT REFERENCE NUMBER	ACROMAG PART NUMBER	DESCRIPTION
U19-34	1033-616	IC H11L1
U61	5024-529(-530)	Programmed part (-L option)
U62	1033-417	TMM2015AP-15
U63	1033-578	IC XC3030-70PC84C
U64	1033-715	IC XC2018-50PC84C
U65	5024-536	Programmed part
R3-18	1100-775	RES NET 2% 9-C0M HIP 10K
R19,20	1100-635	RES NET 2% 9-COM 270 OHM
R30	1000-836	RES FILM 5% .25W 2.7K OHM
C7,8,13,14,31-34	1002-530	CAP MONO 0.1UF 100V Z5U
D19	1001-113	DIODE 1N914B
X2,3	1004-606	CHIP CARRIER, 84 PIN
P4	1004-687	CONN. 32 POS RA PC MOUNT
P9	1004-410	POSTS 1 ROW 2 POS
J7	1004-377	HEADER 8 POST 2 ROW
J9-24	1004-621	HEADER 3 POST SHORT

TABLE 5.2A: PARTS LIST FOR MODEL AVME9440-I-L)
(LED EXPANSION BOARD - PARTS UNIQUE TO THIS MODEL)

COMPONENT REFERENCE NUMBER	ACROMAG PART NUMBER	DESCRIPTION
U1-2	1033-279	IC SN74LS645ND
R1,2	1100-636	RES NET 2% 9-COM 560 OHM
R3,4	1100-490	RES NETWORK 9 1K
C1,2	1002-530	CAP MONO 0.1UF 100V Z5U
D1-16	1001-198	DIODE RED 3MM
D17-32	1001-199	DIODE GREEN 3MM
P1-4	1004-645	SOCKET 9-PIN SINGLE ROW

TABLE 5.2B: PARTS LIST FOR MODEL AVME9443-I-L)
(LED EXPANSION BOARD - PARTS UNIQUE TO THIS MODEL)

COMPONENT REFERENCE NUMBER	ACROMAG PART NUMBER	DESCRIPTION
R1,2	1100-636	RES NET 2% 9-COM 560 OHM
D1-16	1001-198	DIODE RED 3MM
P1-4	1004-645	SOCKET 9-PIN SINGLE ROW

TABLE 5.2C: PARTS LIST FOR MODEL AVME9447-I-L)
(LED EXPANSION BOARD - PARTS UNIQUE TO THIS MODEL)

COMPONENT REFERENCE NUMBER	ACROMAG PART NUMBER	DESCRIPTION
U1-2	1033-279	IC SN74LS645ND
R3,4	1100-490	RES NETWORK 9 1K
C1,2	1002-530	CAP MONO 0.1UF 100V Z5U
D17-32	1001-199	DIODE GREEN 3MM
P1-4	1004-645	SOCKET 9-PIN SINGLE ROW

6.0 SPECIFICATIONS

Operating Temperature	0 to +70 deg. C
Storage Temperature	-25 to +85 deg. C
Relative Humidity	5-95% non-condensing.
Physical Characteristics:	(Double Eurocard)
Length	9.187 in. (233.3 mm)
Width	6.299 in. (160.0 mm)
Board Thickness	0.062 in. (1.59 mm)
Component Height	0.550 in. (13.97 mm)
Recommended Card Spacing	0.800 in. (20.32 mm)

Mating Connectors:

P1	96 pin 603-2-IEC class 2
P2	Not Used
P3,P4	Panduit No. 100-532-033; Type B Male Connectors, rows A & B equipped,even pins only (32 pins total).

Power Requirements:

+ 5 Volts (+/-5%)	1.0A typical, 1.5A maximum
+ 12 Volts	0.0mA (no load)

VME COMPLIANCE

Meets or exceeds all written VME specifications per revision C.1 dated October, 1985 and IEC 821-1987.

Data Transfer Bus	A24/A16:D16/D08 (EO) DTB slave
VMEbus Access Time	580nS typical (all registers) (Measured from the falling edge of DSx* to the falling edge of DTACK*.)
Address Modifier Codes	29H, 2DH, 39H, 3DH
Memory Map	Standard or short address space; Supervisory or non-privileged access; Occupies 1K byte; Base address jumper-selectable; InterruptsI(1-7) request levels; single or multiple interrupt vectors; D08 (O) interrupter; Release On Register Access type (RORA); user control of priority, sense and enable

DIGITAL INPUTS

Input Points per Card	16 (9440-I & 9447-I)
Input Voltage Ranges	2 Selectable Ranges (via jumper): 4-25V DC; 20-55V DC
Input Threshold	4V DC maximum (4-25V DC range); 20V DC maximum (20-55V DC range)

Input Current..18.4mA DC typ. @ 25V (4-25V DC range)
4.7mA DC typ. @ 55V (20-55V DC range)
Input Optical Gate Response Time..1uS. typ. (7uS. maximum)
Input Debounce Time (See Note 1).......................................4 Selectable Ranges (via jumper):
7-8uS. (1 MHz. debounce clock)
336 to 384uS. (20.83KHz. clock)
672 to 768uS. (10.415KHz. clock)
1.344 to 1.536mS. (5.208KHz. clock)
Input Data Register Response Time.......................................1uS. to 192uS. (See Note 2)
Total Input Channel Response Time.......................................9uS. to 1.74mS. (See Note 3)
Logic Compatibility...Can be interfaced to TTL and CMOS (See Section 2.7)
Input "ON" Indicating LEDs...16 green LEDs (front panel) (driven by the optical gate outputs) (with -L option only)

NOTE 1: Input Debounce times are derived by multiplying the period of the selected debounce clock by 7 to 8 (i.e. 1 tick of uncertainty).

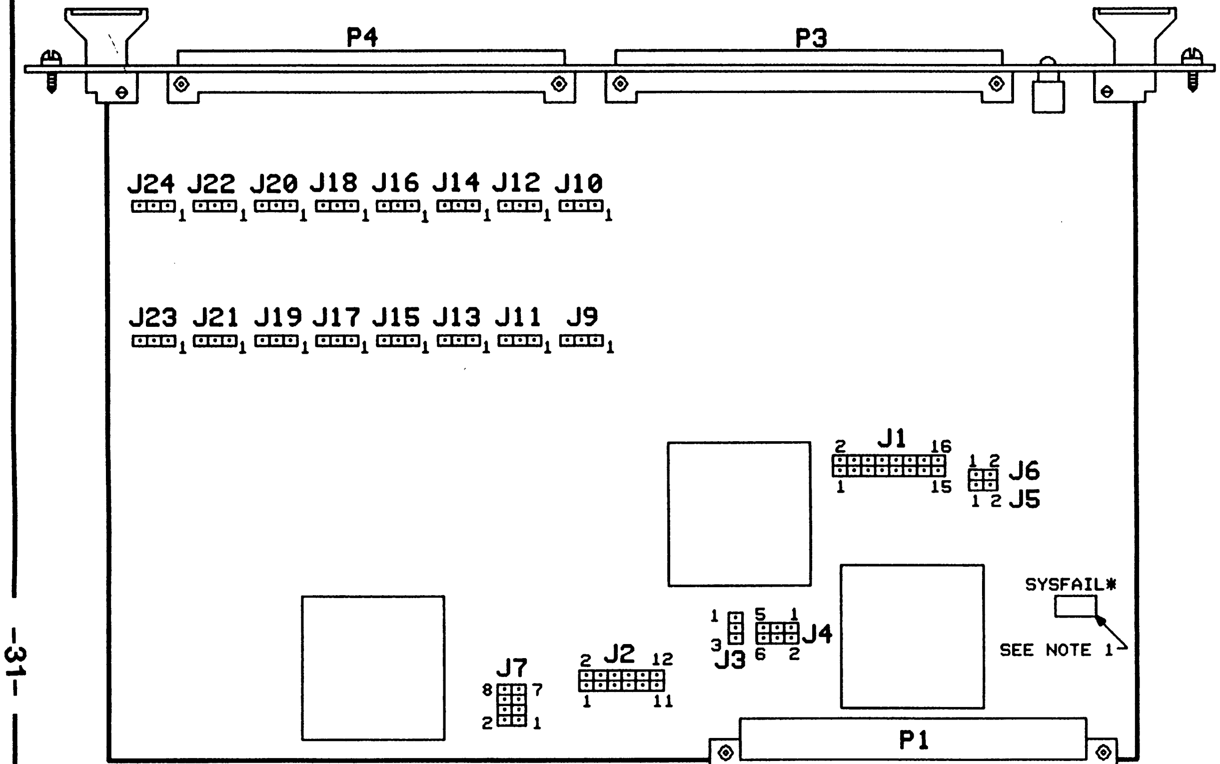
NOTE 2: Input Data Register Response time is derived by multiplying the period of the selected debounce clock by one.

NOTE 3: Total Input Channel Response time is calculated by summing the input optical gate, debounce, and data register response times for the debounce clock selected.

DIGITAL OUTPUTS

Output Points per Card.. 16 (9440-I & 9443-I)
Output Type... Solid State Relay (SSR) Form A (SPST - NO) (Single Pole Single Throw - Normally Open)
Output "OFF" Voltage Range.. 0 to +55V DC (in a single range)
Output "OFF" Leakage Current .... 5uA. DC maximum @ 55V DC
Output "ON" Current Range.. 0 to +1 Amp DC (0 to 40 deg. C)
Derate "ON" Current Above 40 C... 10mA. per deg. C
Output "ON" Voltage @ 1 Amp DC.. 0.5V DC maximum
Output Response Time @ 1 Amp DC..................................... 2.0mS. maximum
Logic Compatibility... Can be interfaced to TTL and CMOS (See Section 2.7)
Output Fuse.. F1-16 (PICO 2 AMP, No. 255002)
Output "ON" Indicating LEDs.. 16 red LEDs (front panel) (driven by the input signal to the SSR) (with -L option only)

ISOLATION VOLTAGE... Between individual digital I/O channels and between all digital I/O channels and the VMEbus: 250V AC or 354V DC on a continuous basis (will withstand 1500V AC dielectric strength test for one minute without breakdown). Complies with test requirements outlined in ANSI C39.5-1974 for the voltage rating specified.



J1: ADDRESS DECODE JUMPER CONFIGURATION

	PINS OF J1							
BASE ADDRESS	A23 15 & 16	A22 13 & 14	A21 11 & 12	A20 9 & 10	A19 7 & 8	A18 5 & 6	A17 3 & 4	A16 1 & 2
00000000H	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
00010000H	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN
00020000H	OUT	OUT	OUT	OUT	OUT	OUT	IN	OUT
00030000H	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN
• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •
00FC0000H	IN	IN	IN	IN	IN	IN	OUT	OUT
00FD0000H	IN	IN	IN	IN	IN	IN	OUT	IN
00FE0000H	IN	IN	IN	IN	IN	IN	IN	OUT
00FF0000H	IN	IN	IN	IN	IN	IN	IN	IN

J2: ADDRESS DECODE JUMPER CONFIGURATION

	PINS OF J2					
BASE ADDRESS	A15 11 & 12	A14 9 & 10	A13 7 & 8	A12 5 & 6	A11 3 & 4	A10 1 & 2
00000000H	OUT	OUT	OUT	OUT	OUT	OUT
00000400H	OUT	OUT	OUT	OUT	OUT	IN
00000800H	OUT	OUT	OUT	OUT	IN	OUT
00000C00H	OUT	OUT	OUT	OUT	IN	IN
00001000H	OUT	OUT	OUT	IN	OUT	OUT
• • •	• • •	• • •	• • •	• • •	• • •	• • •
0000EC00H	IN	IN	IN	OUT	IN	IN
0000F000H	IN	IN	IN	IN	OUT	OUT
0000F400H	IN	IN	IN	IN	OUT	IN
0000F800H	IN	IN	IN	IN	IN	OUT
0000FC00H	IN	IN	IN	IN	IN	IN

J4: BOARD INTERRUPT LEVEL SELECTION

INTERRUPT LEVEL	J4 5 & 6	J4 3 & 4	J4 1 & 2
NONE	OUT	OUT	OUT
1	OUT	OUT	IN
2	OUT	IN	OUT
3	OUT	IN	IN
4	IN	OUT	OUT
5	IN	OUT	IN
6	IN	IN	OUT
7	IN	IN	IN

J9-J24: DIGITAL INPUT THRESHOLD SELECTION

CHANNEL RANGE	J9-J24 1 & 2	J9-J24 2 & 3	POSITIVE THRESHOLD VOLTAGE (MAXIMUM)
4-25V DC	OUT	IN	4V DC
20-55V DC	IN	OUT	20V DC

J3, J5, J6: ADDRESS MODIFIER JUMPER CONFIGURATION

	PINS OF J3,J5,J6			
J3 1 & 2	J3 2 & 3	J5 1 & 2	J6 1 & 2	ADDRESS MODIFIER CODE/FUNCTION
OUT	IN	OUT	IN	2DH ONLY SHORT SUPERVISORY ACCESS
OUT	IN	IN	IN	2DH & 29H SHORT SUPERVISORY ACCESS AND SHORT NON-PRIVILEGED ACCESS
IN	OUT	OUT	OUT	3DH ONLY STANDARD SUPERVISORY DATA ACCESS
IN	OUT	IN	OUT	3DH & 39H STANDARD SUPERVISORY DATA ACCESS AND STANDARD NON-PRIVILEGED DATA ACCESS

J7: DEBOUNCE DELAY SELECTION

DEBOUNCE DELAY TIME (µS)	J7 1 & 2	J7 3 & 4	J7 5 & 6	J7 7 & 8
7 TO 8	OUT	OUT	OUT	IN
336 TO 384	OUT	OUT	IN	OUT
672 TO 768	OUT	IN	OUT	OUT
1344 TO 1536	IN	OUT	OUT	OUT

NOTE 1: SYSFAIL* CAN BE MADE JUMPER SELECTABLE BY CUTTING A FOIL BETWEEN TWO PADS ON THE SOLDER SIDE AND INSTALLING A BERG HEADER.

AcroMag® WIXOM, MICH. | 30 MAY 91 | TAV JGV
TITLE: JUMPER LOCATION
SIZE: D | SERIES: AVME944x | SHEET: 1 OF 1 | DRAWING: 4501-130

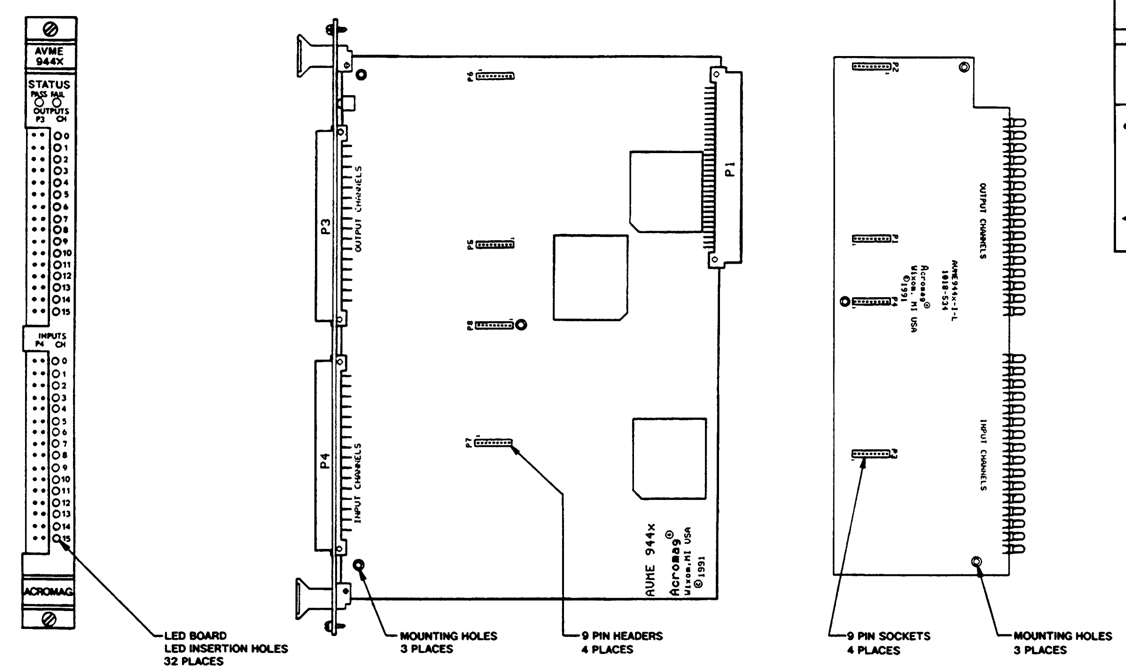
FIGURE 2.1: AVME944x JUMPER LOCATION

Acromag®
WIXOM, MICH.

8 NOV 91

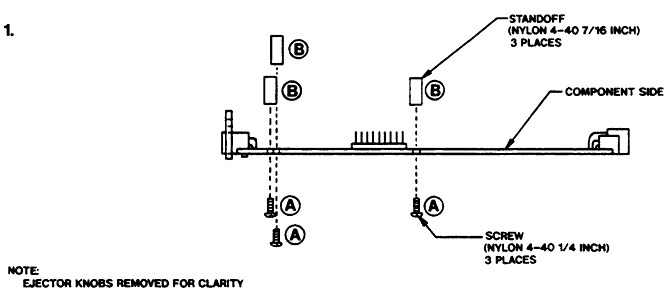
TITLE: LED BOARD TO MAIN BOARD MECHANICAL ASSEMBLY

D | AVME944x | 1 of 1 | 4501-125



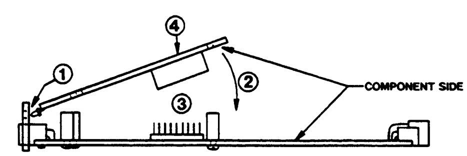
AVME944x FRONT PANEL | **AVME944x MAIN BOARD** | **AVME944x LED BOARD**

STEP 1.



① INSERT NYLON SCREWS, ITEM A, THRU MAIN BOARD INTO SPACERS, ITEM B, (3 PLACES) AND TIGHTEN.

STEP 2.



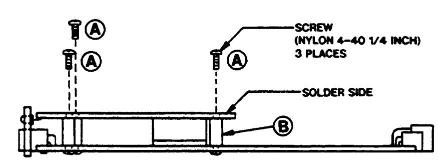
① INSERT LED BOARD'S LEDS INTO FRONT PANEL LED INSERTION HOLES.

② ROTATE LED BOARD TOWARDS MAIN BOARD.

③ CAREFULLY ALIGN FOUR (4) 9 PIN SOCKETS TO FOUR (4) 9 PIN HEADERS.

④ GENTLY PRESS LED BOARD ONTO MAIN BOARD UNTIL SOCKETS AND HEADERS ARE SEATED

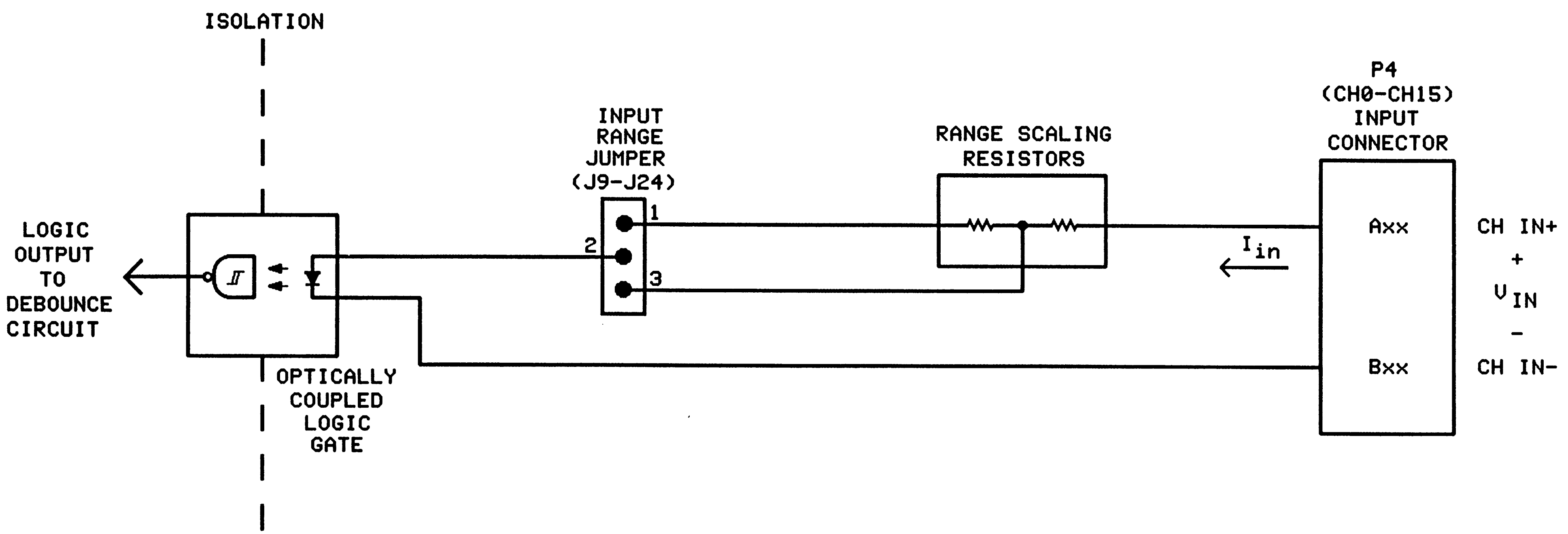
STEP 3.



① INSERT NYLON SCREWS, ITEM A, THRU LED BOARD INTO SPACERS, ITEM B, (3 PLACES) AND TIGHTEN.

FIGURE 2.2: AVME 944x LED BOARD TO MAIN BOARD MECHANICAL ASSEMBLY *

* FOLLOW STEPS IN REVERSE ORDER FOR DISASSEMBLY.



RANGES:

944X MODULE RANGE	944X J9-J24 POSITION	944X Iin @MAX VIN
4-25VDC	2-3	18.4mA DC
20-55VDC	1-2	4.7mA DC

FIGURE 2.3: AVME944x SIMPLIFIED DIGITAL INPUT POINT SCHEMATIC

AcroMag® WIXOM, MICH.
30 MAY 91 — TAV JGV —
DATE RV CS DR ENG CLP
TITLE SIMPLIFIED DIGITAL INPUT POINT SCHEMATIC
SIZE D DWG SERIES AVME944x SHEET 1 OF 1 DRAWING 4501-131 REV

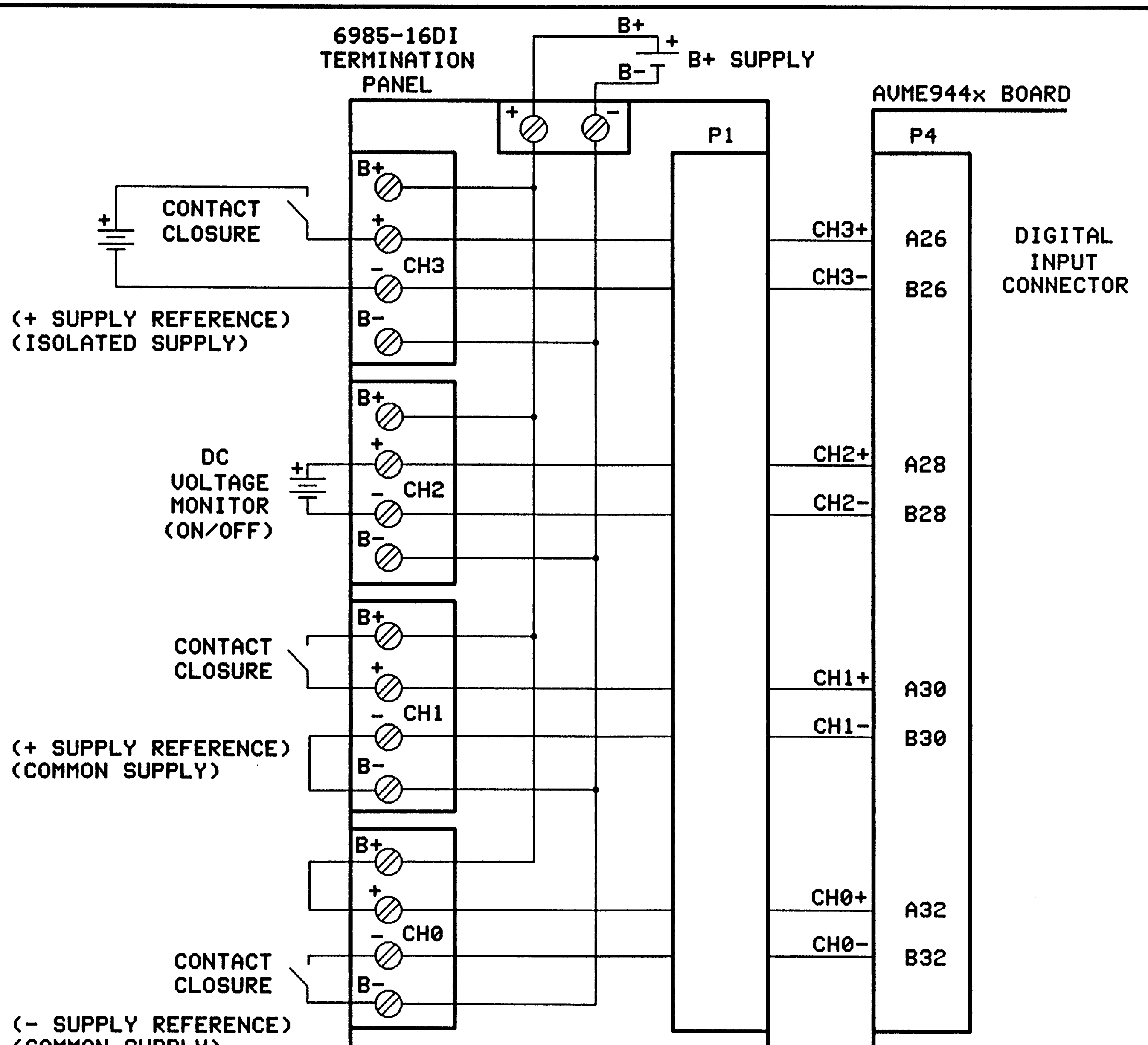
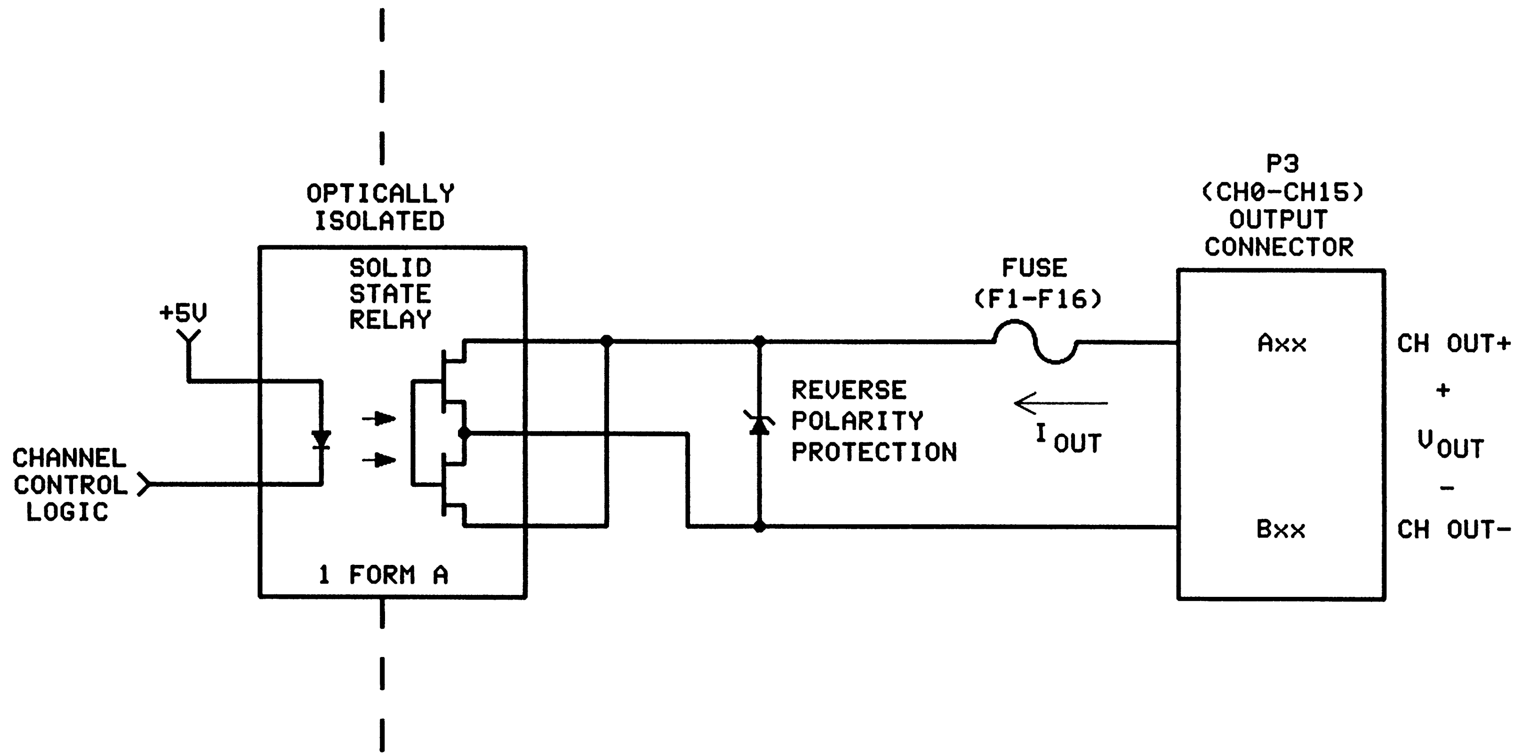


FIGURE 2.4: AVME944x DIGITAL INPUT POINT CONFIGURATIONS

AcroMag® WIXOM, MICH.	30 MAY 91			TAV	JGV	
TITLE	DIGITAL INPUT POINT CONFIGURATIONS					
SIZE D	SERIES AVME944x	SHEET 1 OF 1	DRAWING 4501-132	REV		



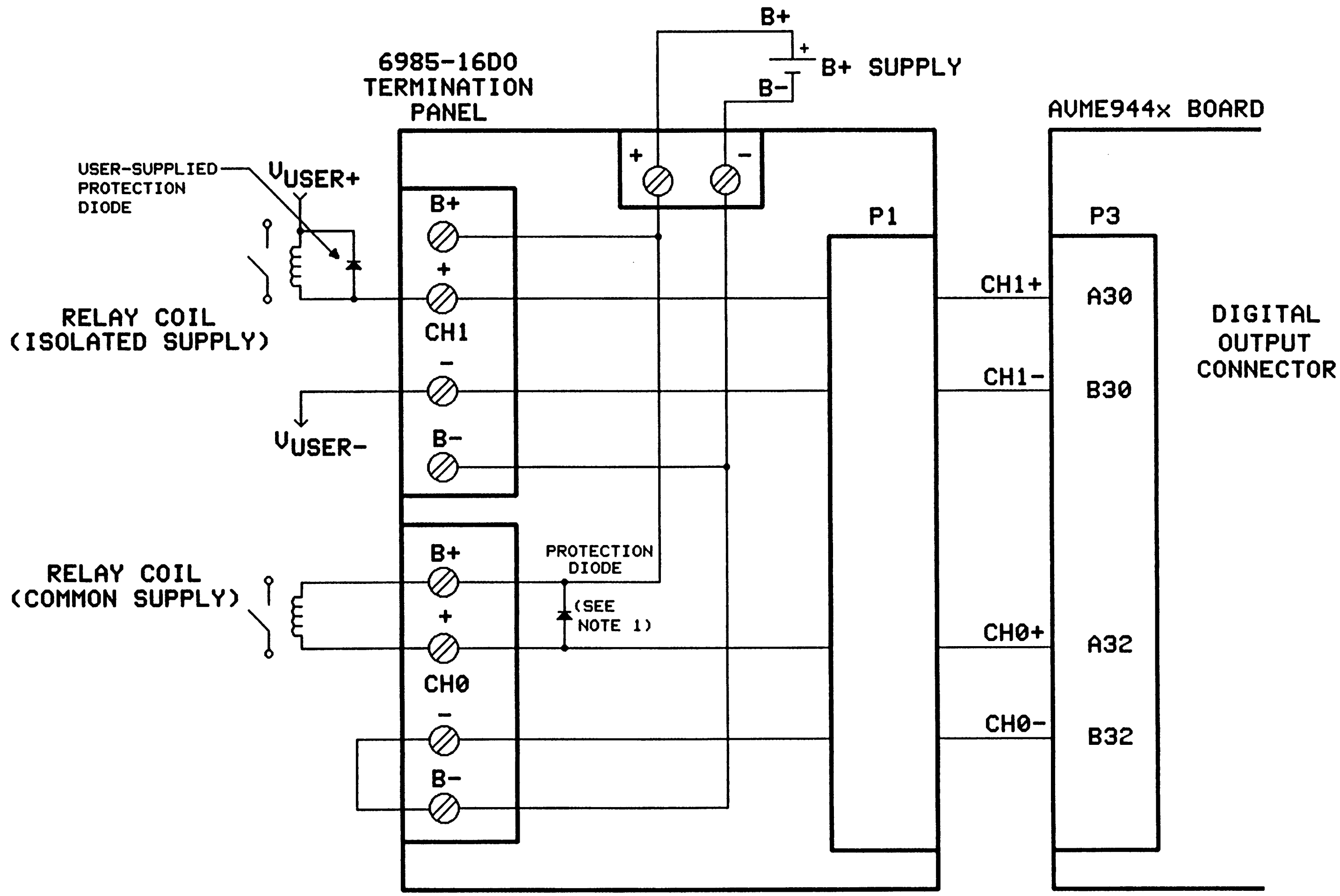
RANGE:

MAX V_{OUT} = 55VDC (SWITCH OFF)

MAX I_{OUT} = 1A DC (SWITCH ON)

FIGURE 2.5: AVME944x SIMPLIFIED DIGITAL OUTPUT POINT SCHEMATIC

AcroMag® WIXOM, MICH.	30 MAY 91	-	—	TAV	JGV	—
	DATE	RV	CO	DR	ENG	CLP
TITLE	SIMPLIFIED DIGITAL OUTPUT POINT SCHEMATIC					
SIZE D DWG	SERIES AVME944x	SHEET 1 OF 1	DRAWING 4501-133	REV		



NOTE:
1. SLOTS ARE INCLUDED ON THE TERMINATION PANEL TO INSTALL JUMPERS, DIODES, OR RESISTORS FROM B+ TO + (OR B- TO -).

FIGURE 2.6: AVME944x DIGITAL OUTPUT POINT CONFIGURATIONS

Acromag® WIXOM, MICH. | 30 MAY 91 | TAU | JGU
DATE | RV | CE | DR | ENG | CLP
TITLE: DIGITAL OUTPUT POINT CONFIGURATIONS
SIZE: D DWG | SERIES: AVME944x | SHEET: 1 OF 1 | DRAWING: 4501-134 | REV

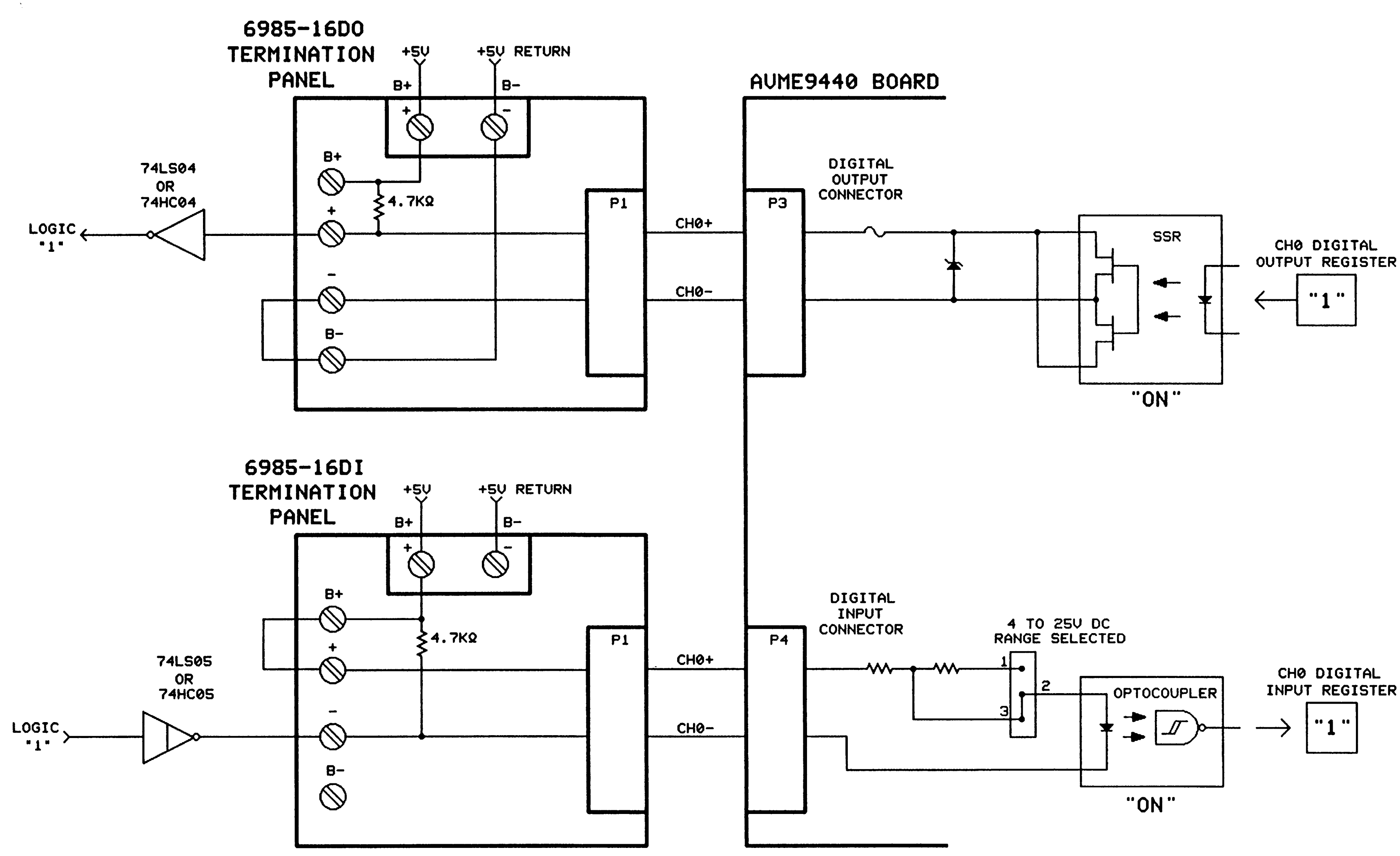
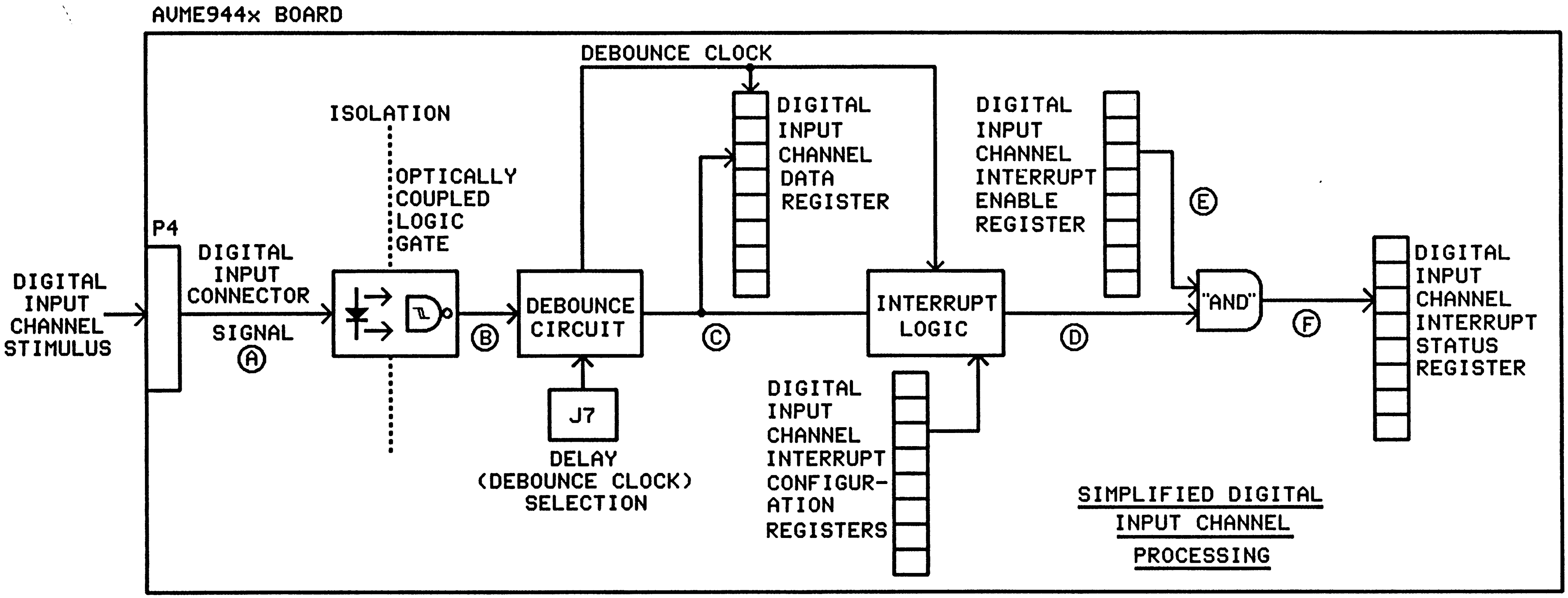


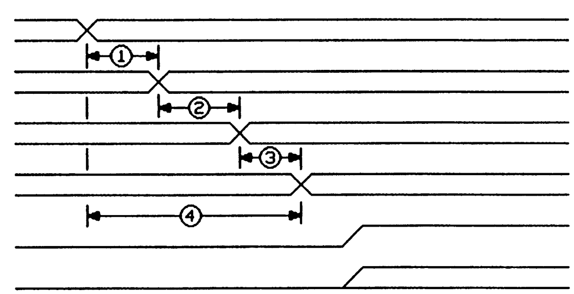
FIGURE 2.7: AVME944x INTERFACE TO TTL AND CMOS SIGNALS

Acromag® WIXOM, MICH.	25 JUL 91 DATE	- RV	—— CB	TAV DR	JGV ENG	— CLP
TITLE	INTERFACE TO TTL AND CMOS SIGNALS					
SIZE D DWG	SERIES AVME944x	SHEET 1 OF 1	DRAWING 4501-137	REV		



SIGNAL	DESCRIPTION
Ⓐ	DIGITAL INPUT CHANNEL STIMULUS (ISOLATED)
Ⓑ	DIGITAL INPUT SIGNAL BUFFERED (NON-ISOLATED)
Ⓒ	DEBOUNCED DIGITAL INPUT SIGNAL
Ⓓ	DIGITAL INPUT CHANNEL INTERRUPT LOGIC SIGNAL
Ⓔ	DIGITAL INPUT CHANNEL INTERRUPT ENABLE
Ⓕ	DIGITAL INPUT CHANNEL INTERRUPT FLAG

INPUT RESPONSE AND INTERRUPT TIMING



① INPUT RESPONSE TIME = 1µS TYP.(7µS MAXIMUM).

② DEBOUNCE DELAY = 7µS TO ~1.54mS (USER SELECTABLE).

③ INTERRUPT LOGIC DELAY = 1µS TO 192µS (FOLLOWS DEBOUNCE CLOCK).

④ TOTAL INPUT RESPONSE TIME = 9µS TO ~1.74mS.

FIGURE 3.3: AVME944x INPUT RESPONSE AND INTERRUPT TIMING DIAGRAM

AcroMag® WIXOM, MICH.

29 JAN 92 | TAU | JGU

TITLE INPUT RESPONSE AND INTERRUPT TIMING DIAGRAM

SIZE D | SERIES AVME944x | SHEET 1 OF 1 | DRAWING 4501-124 | REV

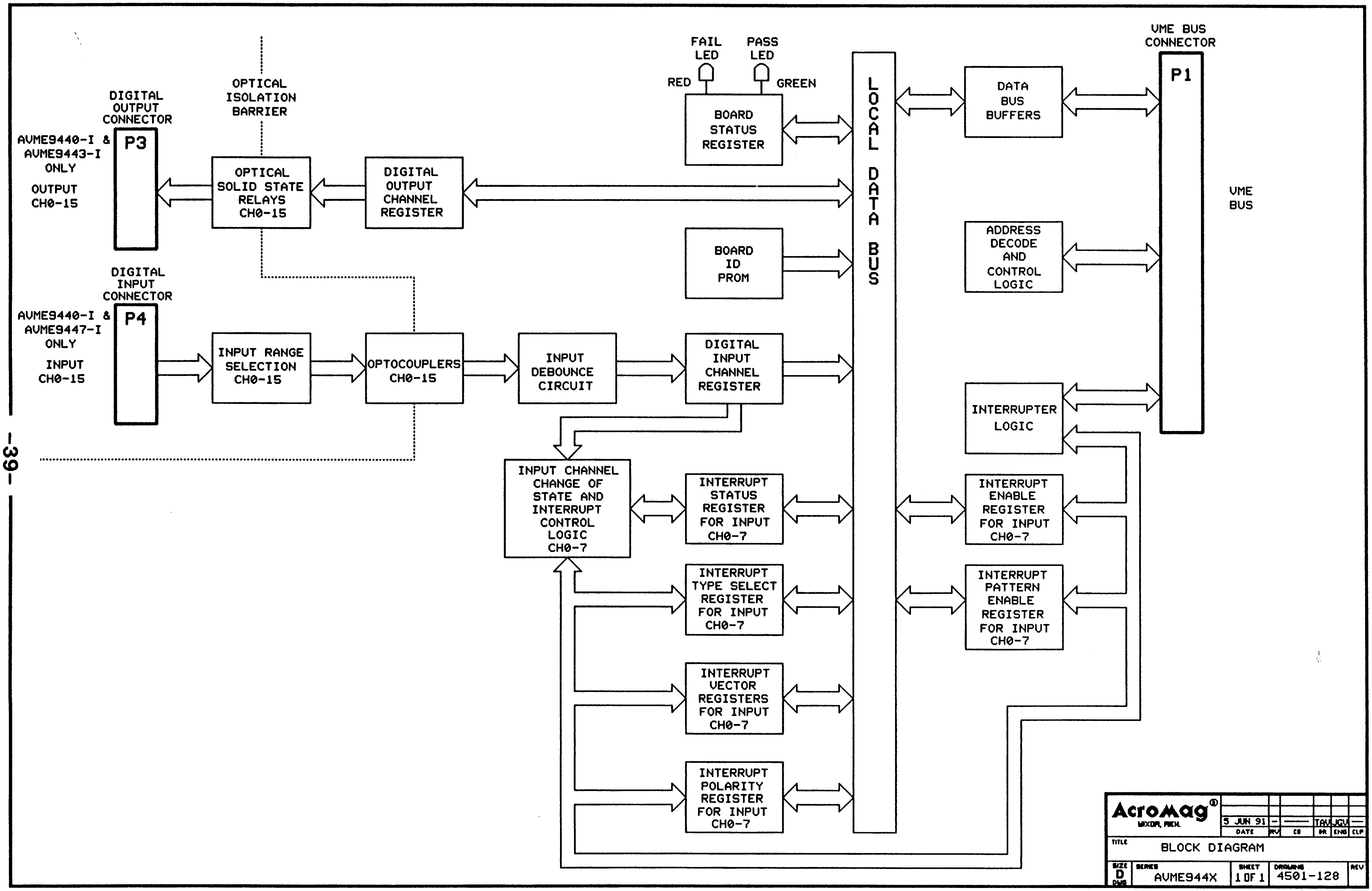
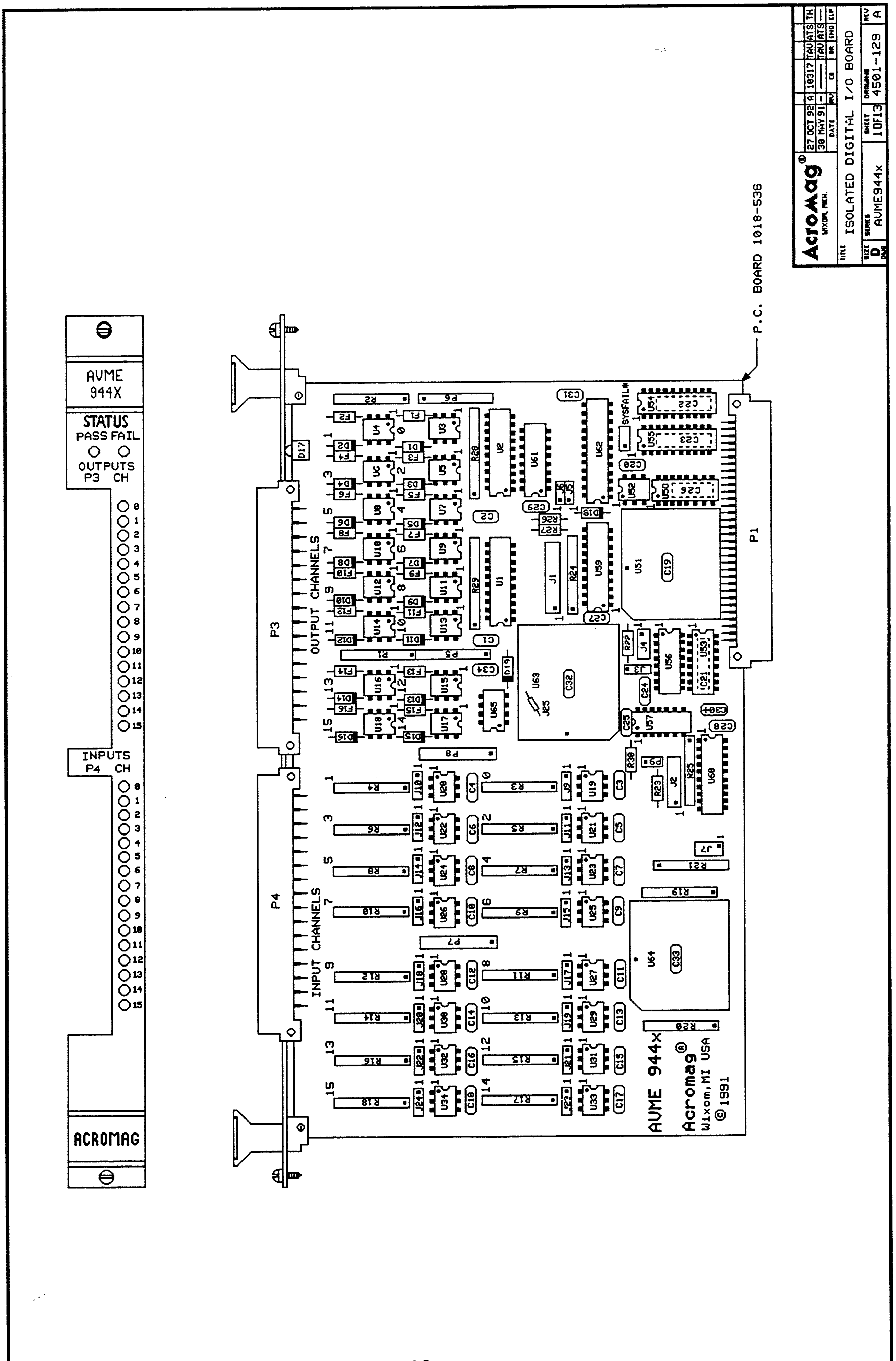
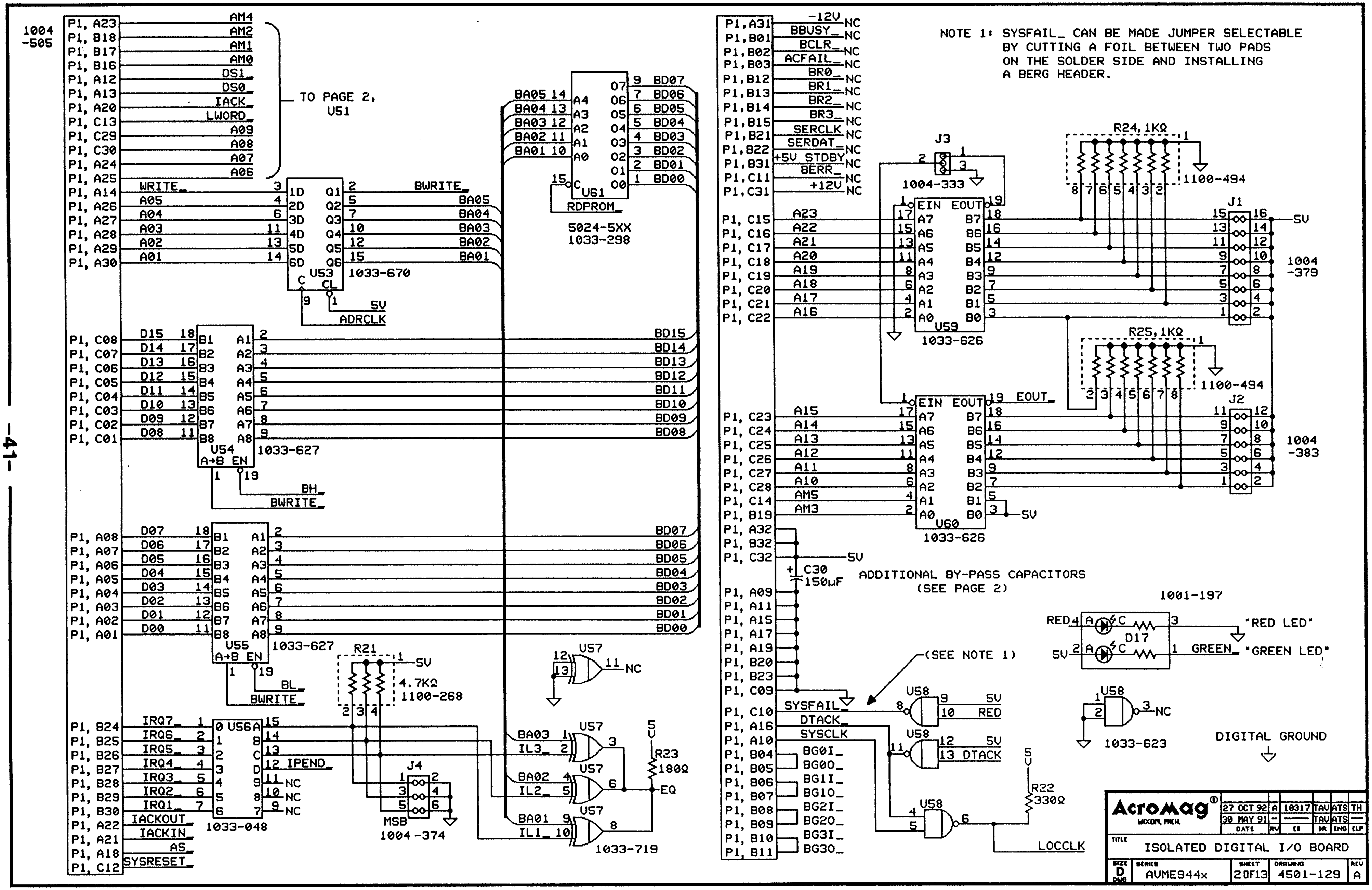
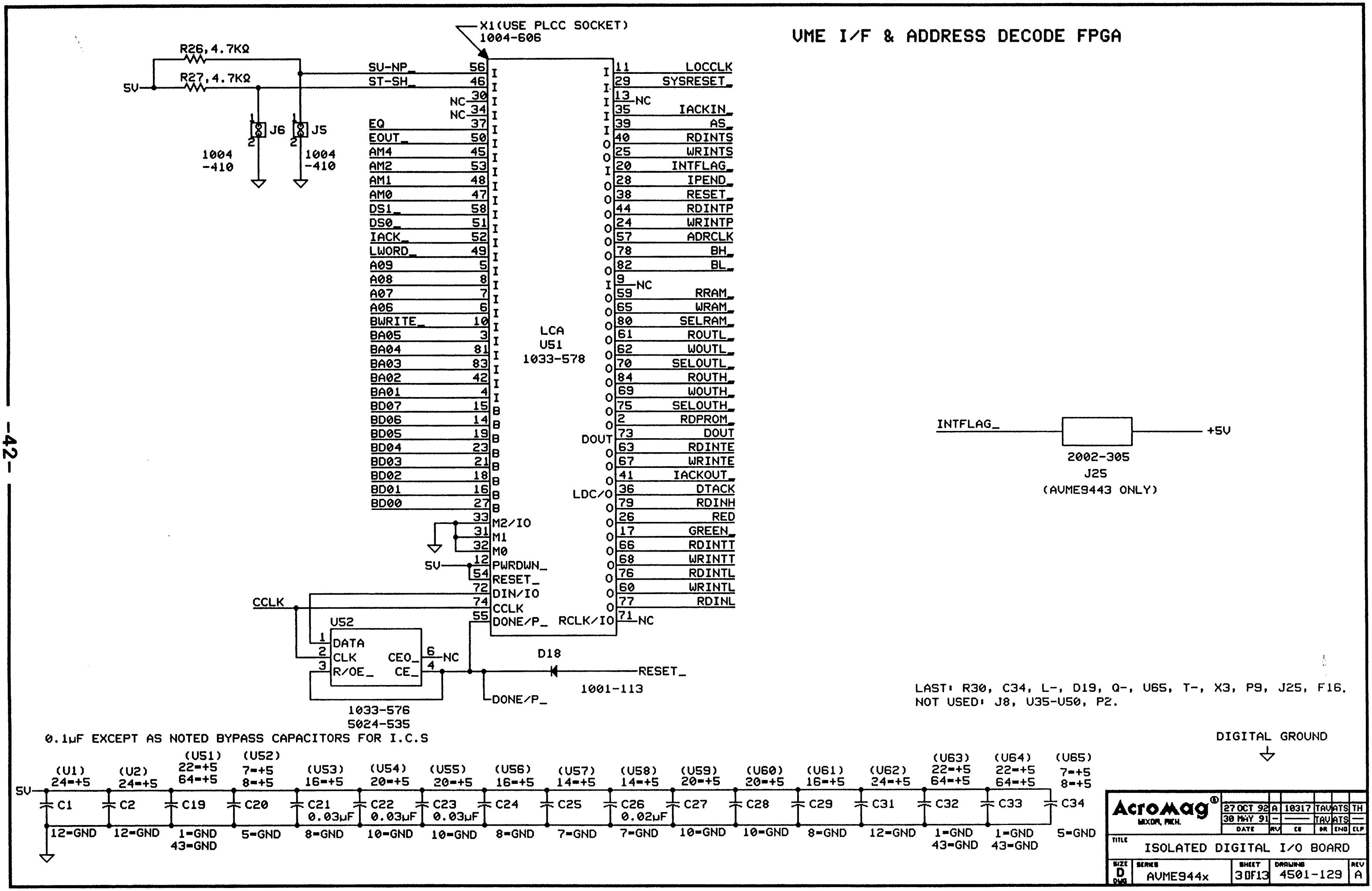


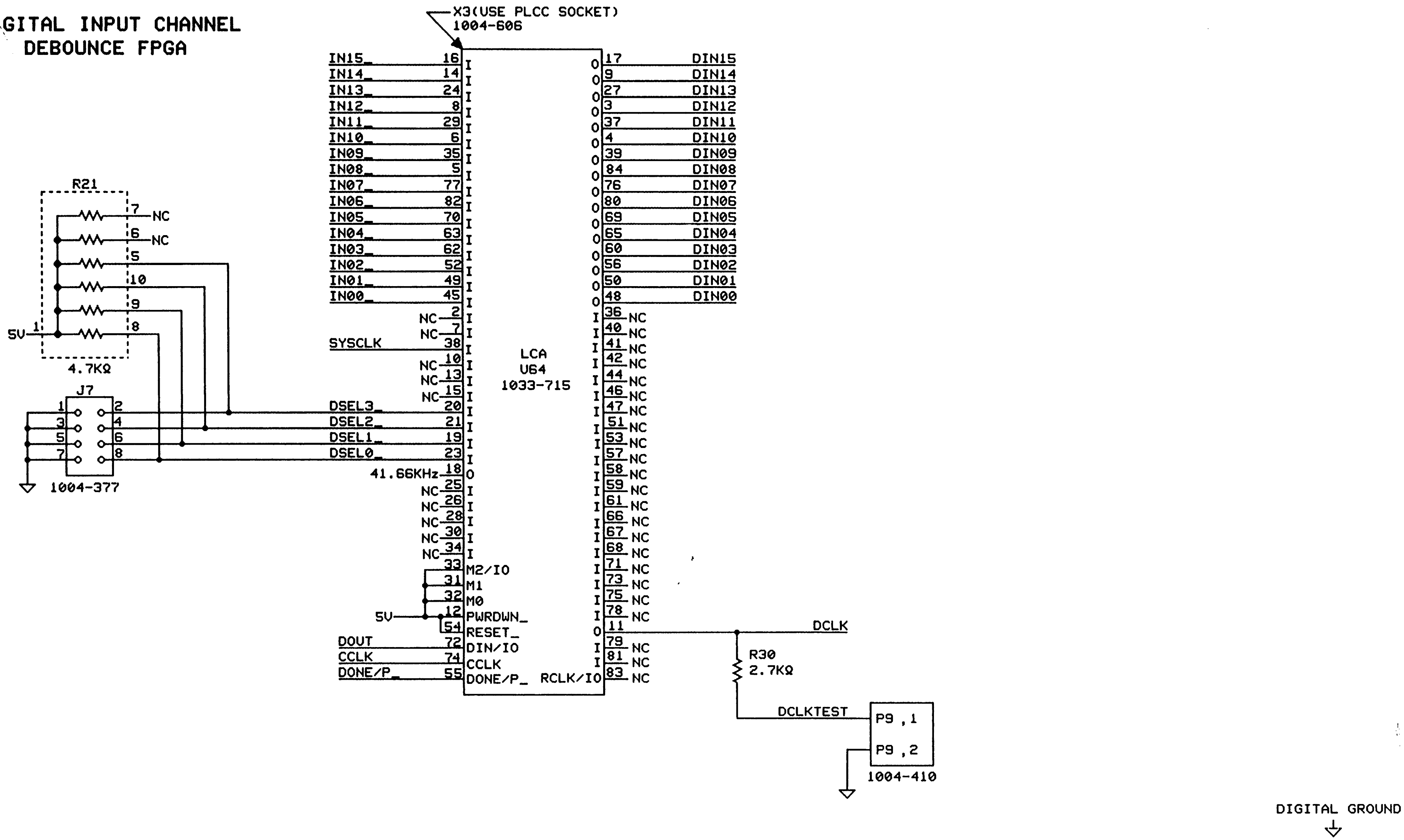
FIGURE 4.1: BLOCK DIAGRAM


AVME
944X
STATUS
PASS FAIL
OUTPUTS
P3 CH
INPUTS
P4 CH
ACROMAG
OUTPUT CHANNELS
INPUT CHANNELS
P3
P4
P1
AVME 944x
Acromag®
Wixom, MI USA
©1991
P.C. BOARD 1018-536
Acromag® WIXOM, MICH.
27 OCT 92 A 10317 TAU ATS TH
30 MAY 91 - TAU ATS
DATE RV CB DR ENG CLP
TITLE ISOLATED DIGITAL I/O BOARD
SIZE D DWG
SERIES AVME944x
SHEET 1 OF 13
DRAWING 4501-129
REV A


NOTE 1: SYSFAIL_ CAN BE MADE JUMPER SELECTABLE
BY CUTTING A FOIL BETWEEN TWO PADS
ON THE SOLDER SIDE AND INSTALLING
A BERG HEADER.
TO PAGE 2, U51
ADDITIONAL BY-PASS CAPACITORS
(SEE PAGE 2)
(SEE NOTE 1)
"RED LED"
"GREEN LED"
DIGITAL GROUND
AcroMag
WIXOM, MICH.
27 OCT 92
30 MAY 91
ISOLATED DIGITAL I/O BOARD
AVME944x
2OF13
4501-129


VME I/F & ADDRESS DECODE FPGA
X1(USE PLCC SOCKET)
1004-606
R26,4.7KΩ
R27,4.7KΩ
5V
J6
J5
1004
-410
1004
-410
SV-NP_ 56
ST-SH_ 46
NC 30
NC 34
EQ 37
EOUT_ 50
AM4 45
AM2 53
AM1 48
AM0 47
DS1_ 58
DS0_ 51
IACK_ 52
LWORD_ 49
A09 5
A08 8
A07 7
A06 6
BWRITE_ 10
BA05 3
BA04 81
BA03 83
BA02 42
BA01 4
BD07 15
BD06 14
BD05 19
BD04 23
BD03 21
BD02 18
BD01 16
BD00 27
33 M2/IO
31 M1
32 M0
5V 12 PWRDWN_
54 RESET_
72 DIN/IO
CCLK 74 CCLK
55 DONE/P_
RCLK/IO
LCA
U51
1033-578
11 LOCCLK
29 SYSRESET_
13 NC
35 IACKIN_
39 AS_
40 RDINTS
25 WRINTS
20 INTFLAG_
28 IPEND_
38 RESET_
44 RDINTP
24 WRINTP
57 ADRCLK
78 BH_
82 BL_
9 NC
59 RRAM_
65 WRAM_
80 SELRAM_
61 ROUTL_
62 WOUTL_
70 SELOUTL_
84 ROUTH_
69 WOUTH_
75 SELOUTH_
2 RDPROM_
DOUT 73 DOUT
63 RDINTE
67 WRINTE
41 IACKOUT_
LDC/O 36 DTACK
79 RDINH
26 RED
17 GREEN_
66 RDINTT
68 WRINTT
76 RDINTL
60 WRINTL
77 RDINL
71 NC
U52
1 DATA
2 CLK
3 R/OE_
CEO_ 6 NC
CE_ 4
1033-576
5024-535
D18
RESET_
1001-113
DONE/P_
INTFLAG_
+5V
2002-305
J25
(AVME9443 ONLY)
LAST: R30, C34, L-, D19, Q-, U65, T-, X3, P9, J25, F16.
NOT USED: J8, U35-U50, P2.
DIGITAL GROUND
0.1µF EXCEPT AS NOTED BYPASS CAPACITORS FOR I.C.S
5V
(U1) 24=+5 C1 12=GND
(U2) 24=+5 C2 12=GND
(U51) 22=+5 64=+5 C19 1=GND 43=GND
(U52) 7=+5 8=+5 C20 5=GND
(U53) 16=+5 C21 0.03µF 8=GND
(U54) 20=+5 C22 0.03µF 10=GND
(U55) 20=+5 C23 0.03µF 10=GND
(U56) 16=+5 C24 8=GND
(U57) 14=+5 C25 7=GND
(U58) 14=+5 C26 0.02µF 7=GND
(U59) 20=+5 C27 10=GND
(U60) 20=+5 C28 10=GND
(U61) 16=+5 C29 8=GND
(U62) 24=+5 C31 12=GND
(U63) 22=+5 64=+5 C32 1=GND 43=GND
(U64) 22=+5 64=+5 C33 1=GND 43=GND
(U65) 7=+5 8=+5 C34 5=GND
AcroMag®
WIXOM, MICH.
27 OCT 92 A 10317 TAV ATS TH
30 MAY 91 - TAV ATS
DATE REV CO DR ENG CLP
TITLE ISOLATED DIGITAL I/O BOARD
SIZE D DWG
SERIES AVME944x
SHEET 3 OF 13
DRAWING 4501-129
REV A

DIGITAL INPUT CHANNEL DEBOUNCE FPGA

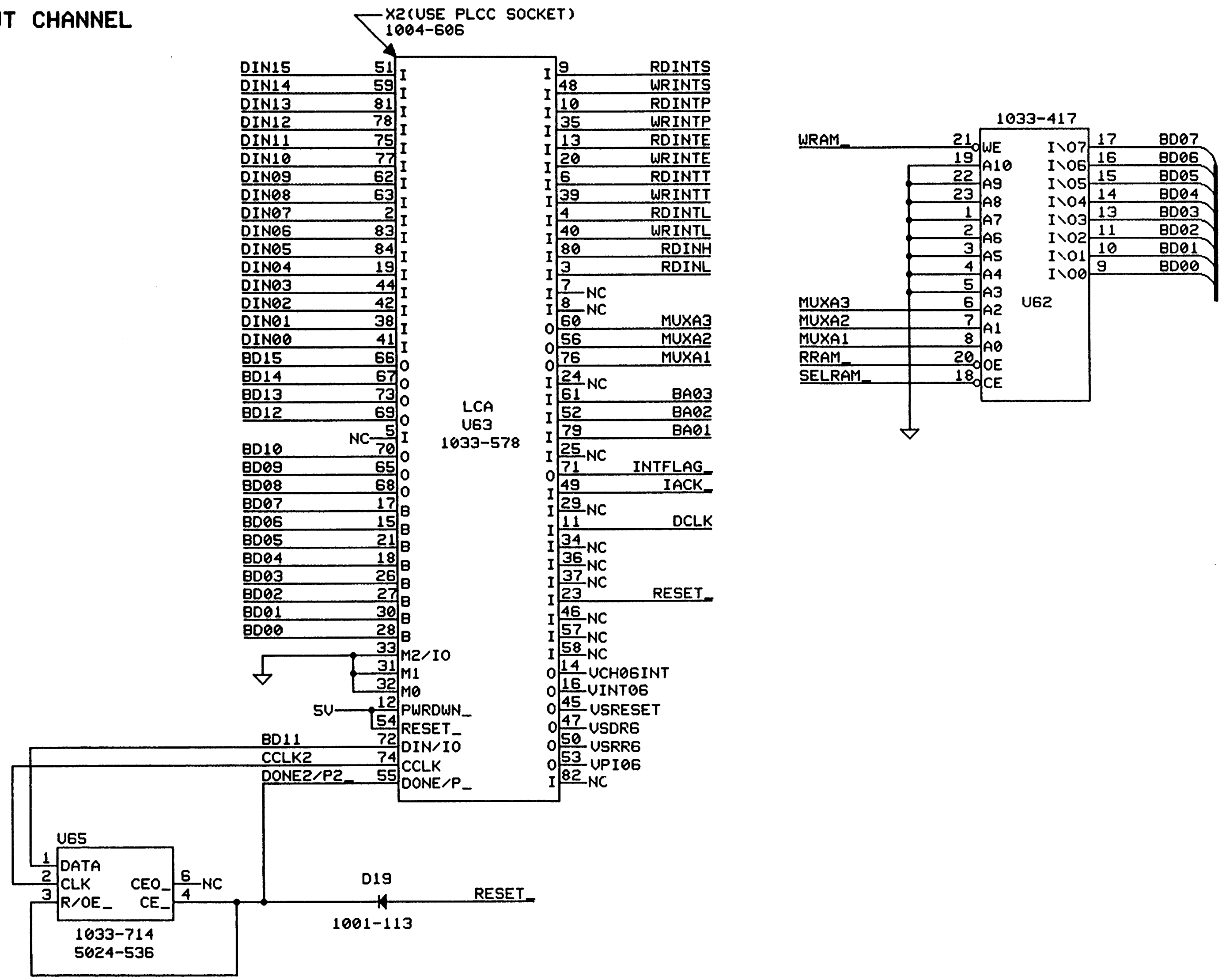


AcroMag® WIXOM, MICH.	27 OCT 92	A	10317	TAV	ATS	TH
	30 MAY 91	-	———	TAV	ATS	—
	DATE	RV	CO	DR	ENG	CLP

TITLE ISOLATED DIGITAL I/O BOARD

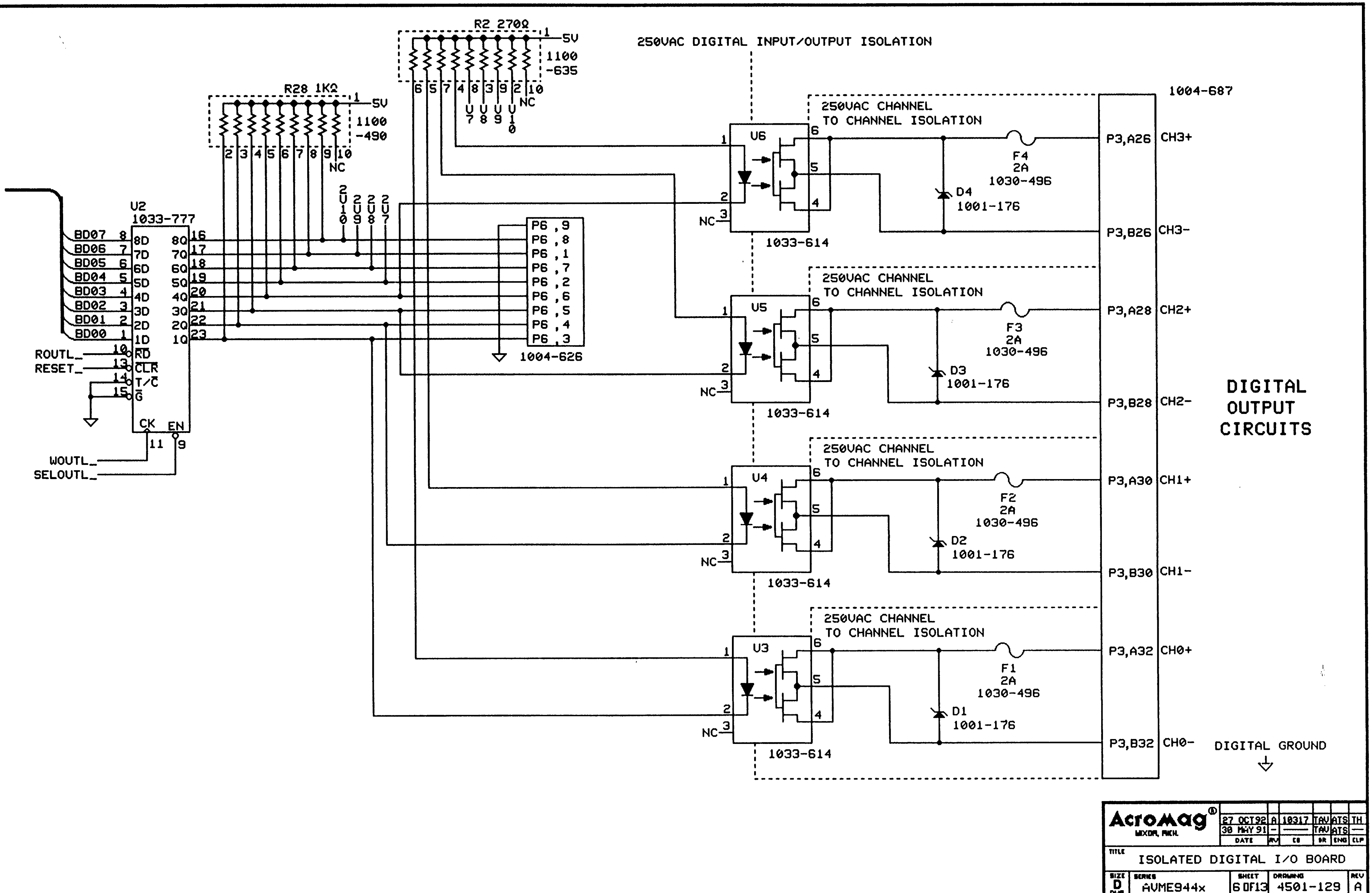
SIZE	SERIES	SHEET	DRAWING	REV
D DWG	AVME944x	4 OF 13	4501-129	A

DIGITAL INPUT CHANNEL
LOGIC FPGA



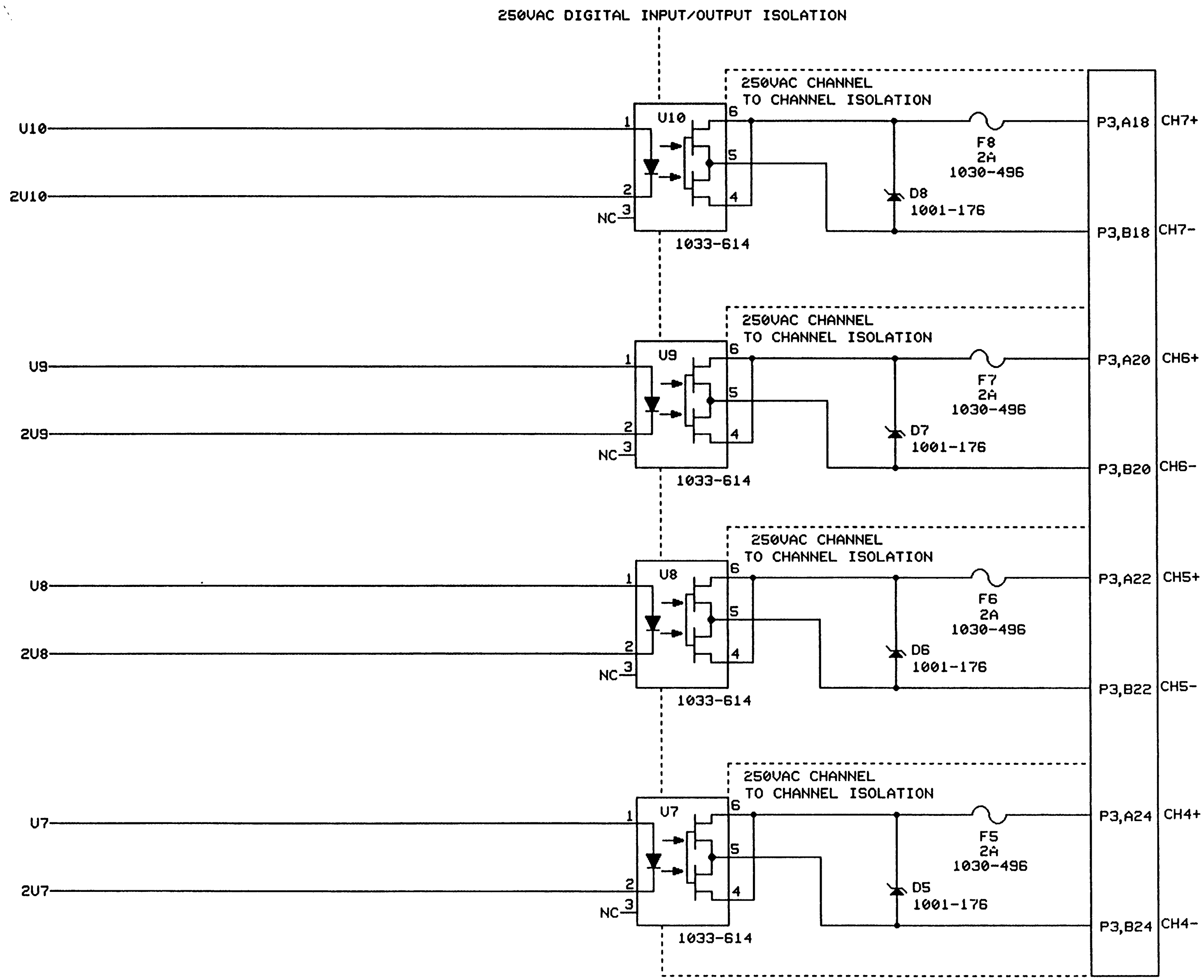
DIGITAL GROUND

AcroMag® WIXOM, MICH.	27 OCT 92	A	10317	TAV	ATS	TH
	30 MAY 91	-	——	TAV	ATS	—
	DATE	RV	EB	DR	ENG	CLP
TITLE ISOLATED DIGITAL I/O BOARD						
SIZE D DWG	SERIES AUME944x	SHEET 5 OF 13	DRAWING 4501-129	REV A		



250VAC DIGITAL INPUT/OUTPUT ISOLATION
250VAC CHANNEL TO CHANNEL ISOLATION
DIGITAL OUTPUT CIRCUITS
R2 270Ω
1100 -635
R28 1KΩ
1100 -490
5V
U2
1033-777
BD07
BD06
BD05
BD04
BD03
BD02
BD01
BD00
ROUTL_
RESET_
WOUTL_
SELOUTL_
1004-626
U6
U5
U4
U3
1033-614
F4
F3
F2
F1
2A
1030-496
D4
D3
D2
D1
1001-176
1004-687
P3,A26 CH3+
P3,B26 CH3-
P3,A28 CH2+
P3,B28 CH2-
P3,A30 CH1+
P3,B30 CH1-
P3,A32 CH0+
P3,B32 CH0-
DIGITAL GROUND
AcroMag WIXOM, MICH.
27 OCT92 A 10317 TAV ATS TH
30 MAY 91 TAV ATS
ISOLATED DIGITAL I/O BOARD
D AVME944x 6 OF 13 4501-129 A

DIGITAL OUTPUT CIRCUITS

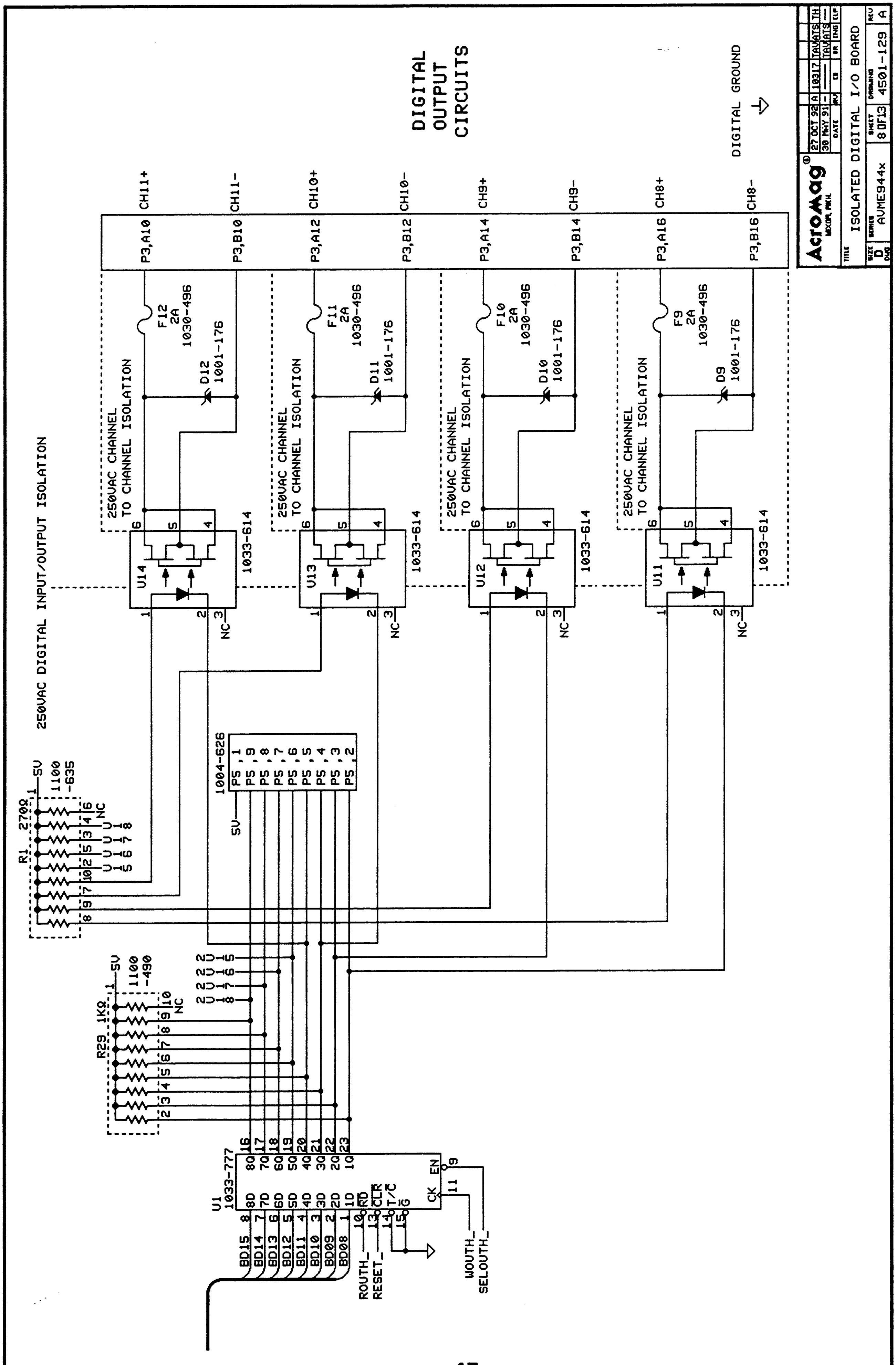


Acromag® WIXOM, MICH.

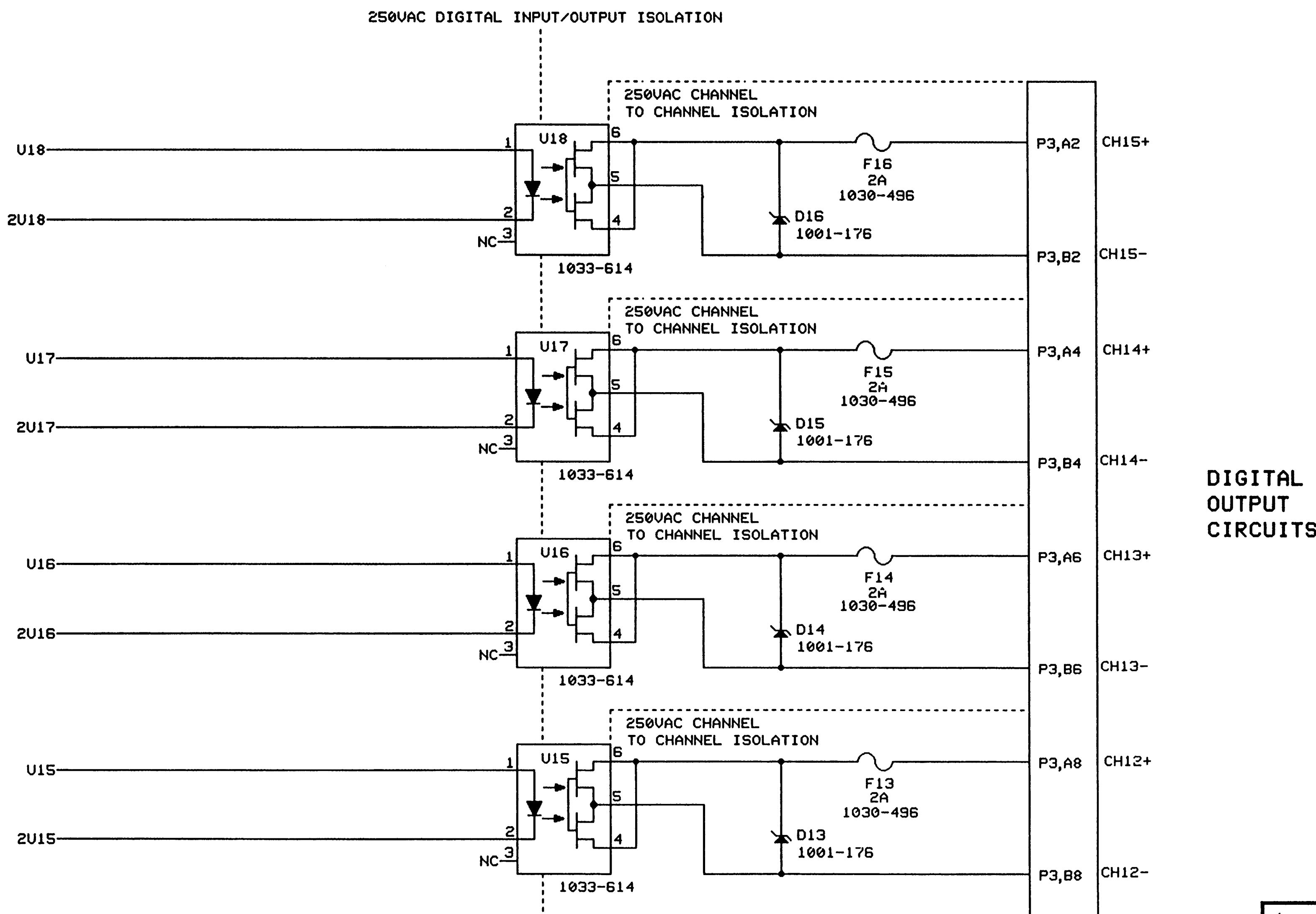
DATE	REV	CO	DR	ENG	CLP
27 OCT 92	A	10317	TAV	ATS	TH
30 MAY 91	-	——	TAV	ATS	—

TITLE ISOLATED DIGITAL I/O BOARD

SIZE	SERIES	SHEET	DRAWING	REV
D DWG	AVME944x	7 OF 13	4501-129	A



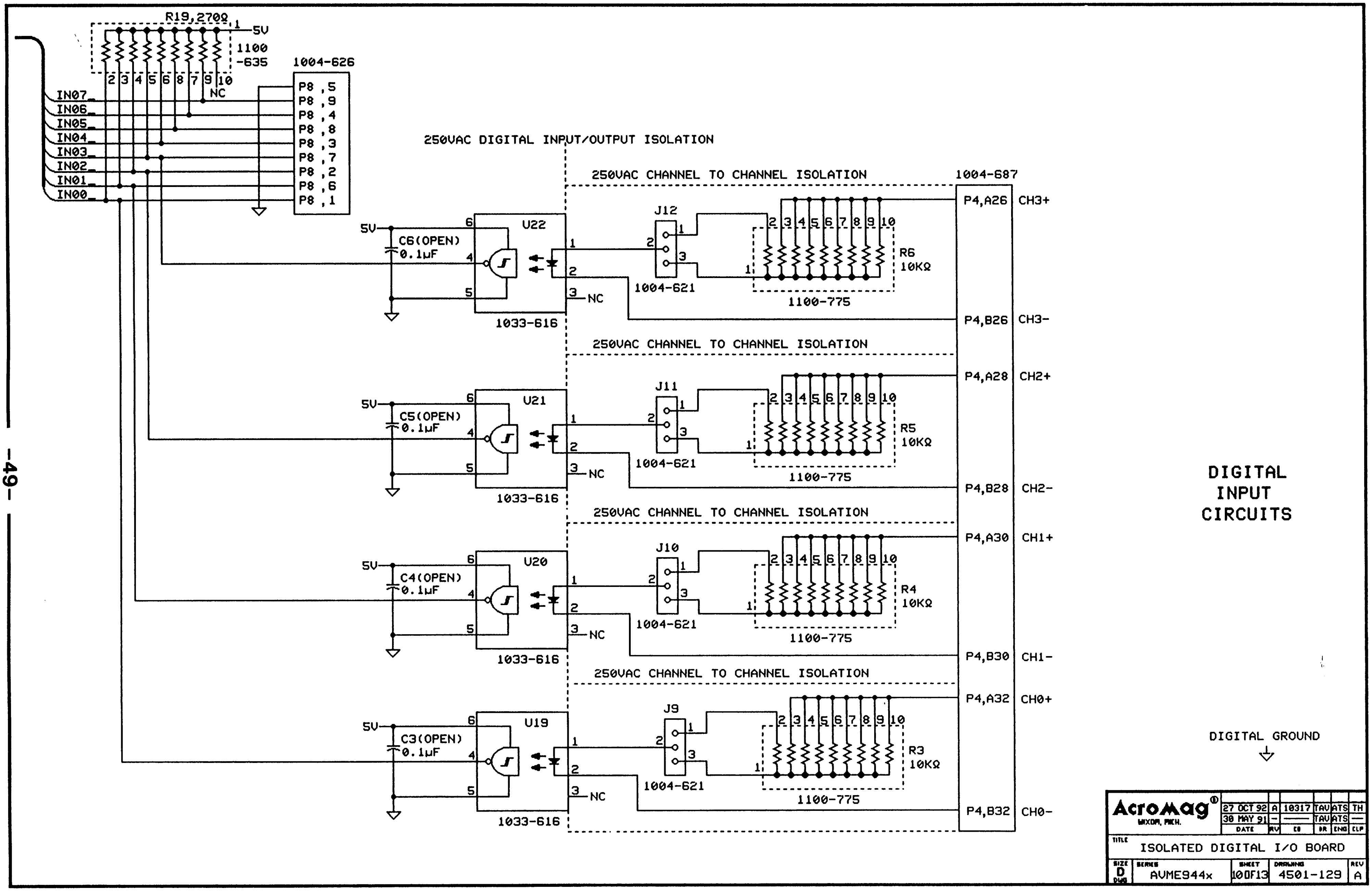
DIGITAL OUTPUT CIRCUITS
DIGITAL GROUND
250VAC DIGITAL INPUT/OUTPUT ISOLATION
250VAC CHANNEL TO CHANNEL ISOLATION
CH11+
CH11-
CH10+
CH10-
CH9+
CH9-
CH8+
CH8-
P3,A10
P3,B10
P3,A12
P3,B12
P3,A14
P3,B14
P3,A16
P3,B16
F12 2A 1030-496
F11 2A 1030-496
F10 2A 1030-496
F9 2A 1030-496
D12 1001-176
D11 1001-176
D10 1001-176
D9 1001-176
U14 1033-614
U13 1033-614
U12 1033-614
U11 1033-614
R1 270Ω 1100-635
R29 1KΩ 1100-490
1004-626
U1 1033-777
BD15
BD14
BD13
BD12
BD11
BD10
BD09
BD08
ROUTH_
RESET_
WOUTH_
SELOUTH_
AcroMag WIXOM, MICH.
ISOLATED DIGITAL I/O BOARD
D AVME944x 8 OF 13 4501-129 A
27 OCT 92
30 MAY 91

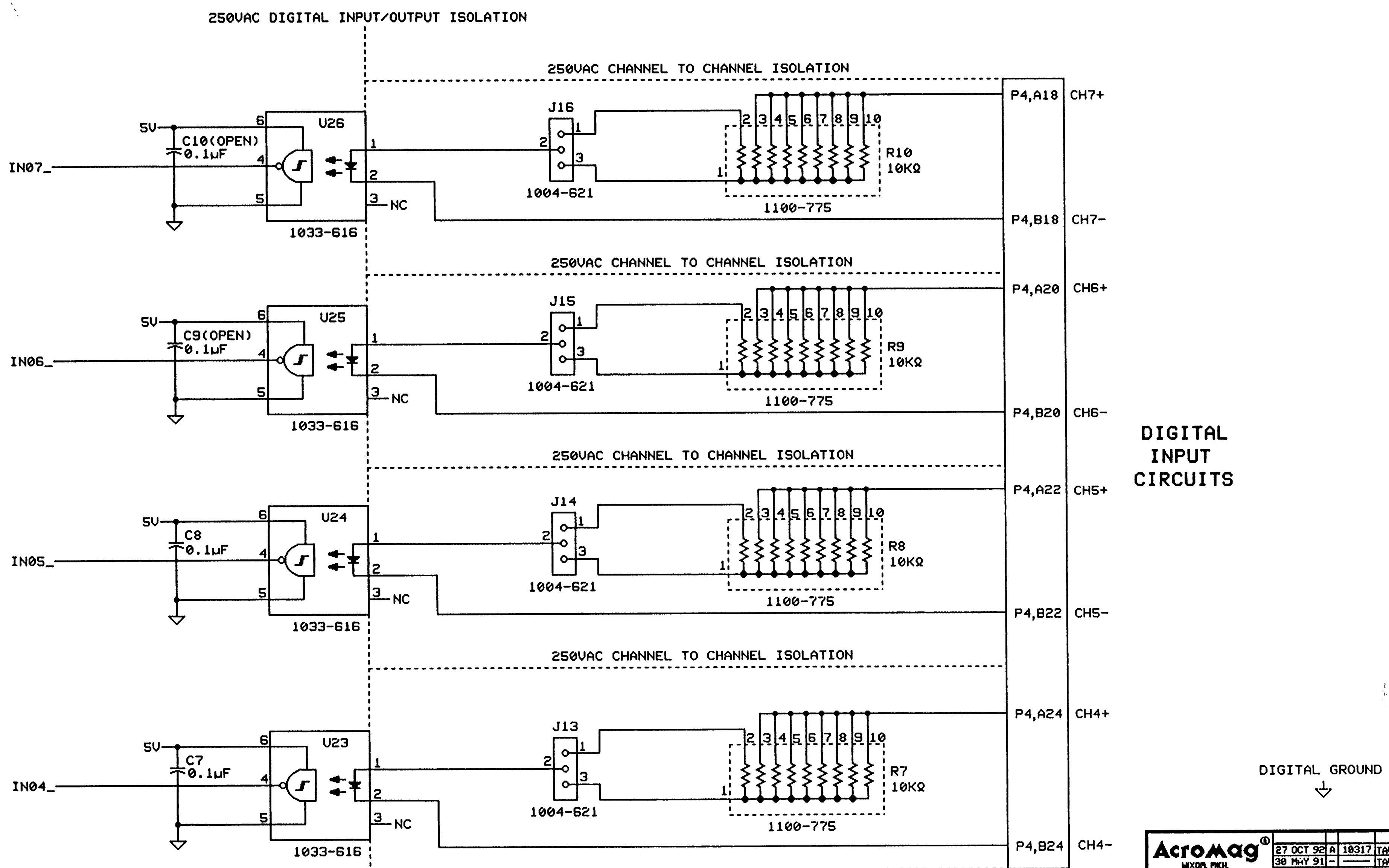


AcroMag® WIXOM, MICH.	27 OCT 92	A	10317	TAV	ATS	TH
	30 MAY 91	-	———	TAV	ATS	—
	DATE	RV	CB	DR	ENG	CLP

TITLE ISOLATED DIGITAL I/O BOARD

SIZE	SERIES	SHEET	DRAWING	REV
D DWG	AVME944x	9 OF 13	4501-129	A


R19,270Ω
5V
1100
-635
1004-626
IN07
IN06
IN05
IN04
IN03
IN02
IN01
IN00
NC
P8 ,5
P8 ,9
P8 ,4
P8 ,8
P8 ,3
P8 ,7
P8 ,2
P8 ,6
P8 ,1
250VAC DIGITAL INPUT/OUTPUT ISOLATION
250VAC CHANNEL TO CHANNEL ISOLATION
1004-687
U22
C6(OPEN)
0.1µF
J12
1004-621
R6
10KΩ
1100-775
1033-616
P4,A26
CH3+
P4,B26
CH3-
U21
C5(OPEN)
0.1µF
J11
R5
10KΩ
P4,A28
CH2+
P4,B28
CH2-
U20
C4(OPEN)
0.1µF
J10
R4
10KΩ
P4,A30
CH1+
P4,B30
CH1-
U19
C3(OPEN)
0.1µF
J9
R3
10KΩ
P4,A32
CH0+
P4,B32
CH0-
DIGITAL
INPUT
CIRCUITS
DIGITAL GROUND
AcroMag
WIXOM, MICH.
27 OCT 92
A
10317
TAV
ATS
TH
30 MAY 91
TAV
ATS
DATE
RV
EB
DR
ENG
CLP
TITLE
ISOLATED DIGITAL I/O BOARD
SIZE
D
DWG
SERIES
AVME944x
SHEET
10OF13
DRAWING
4501-129
REV
A

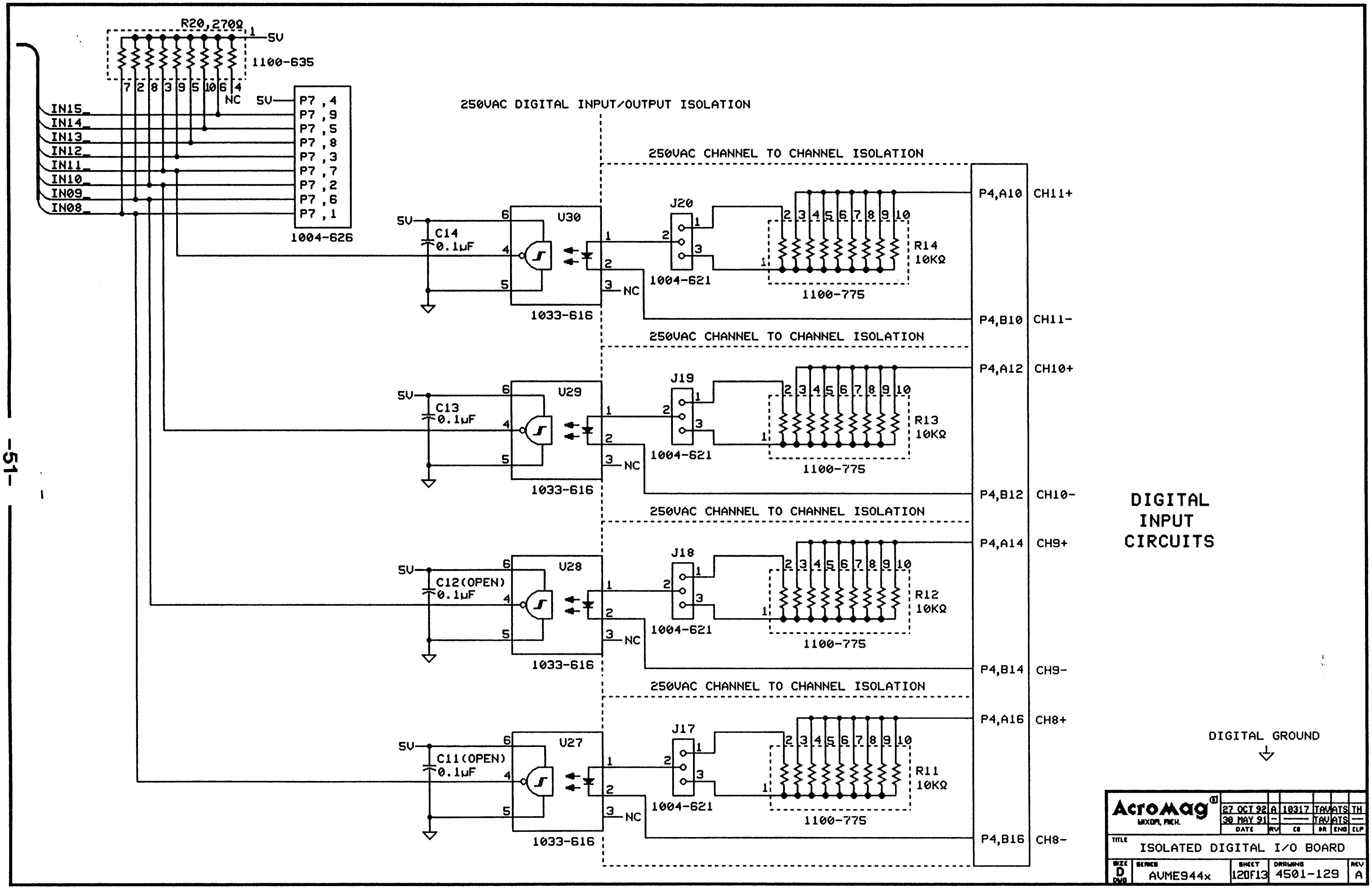


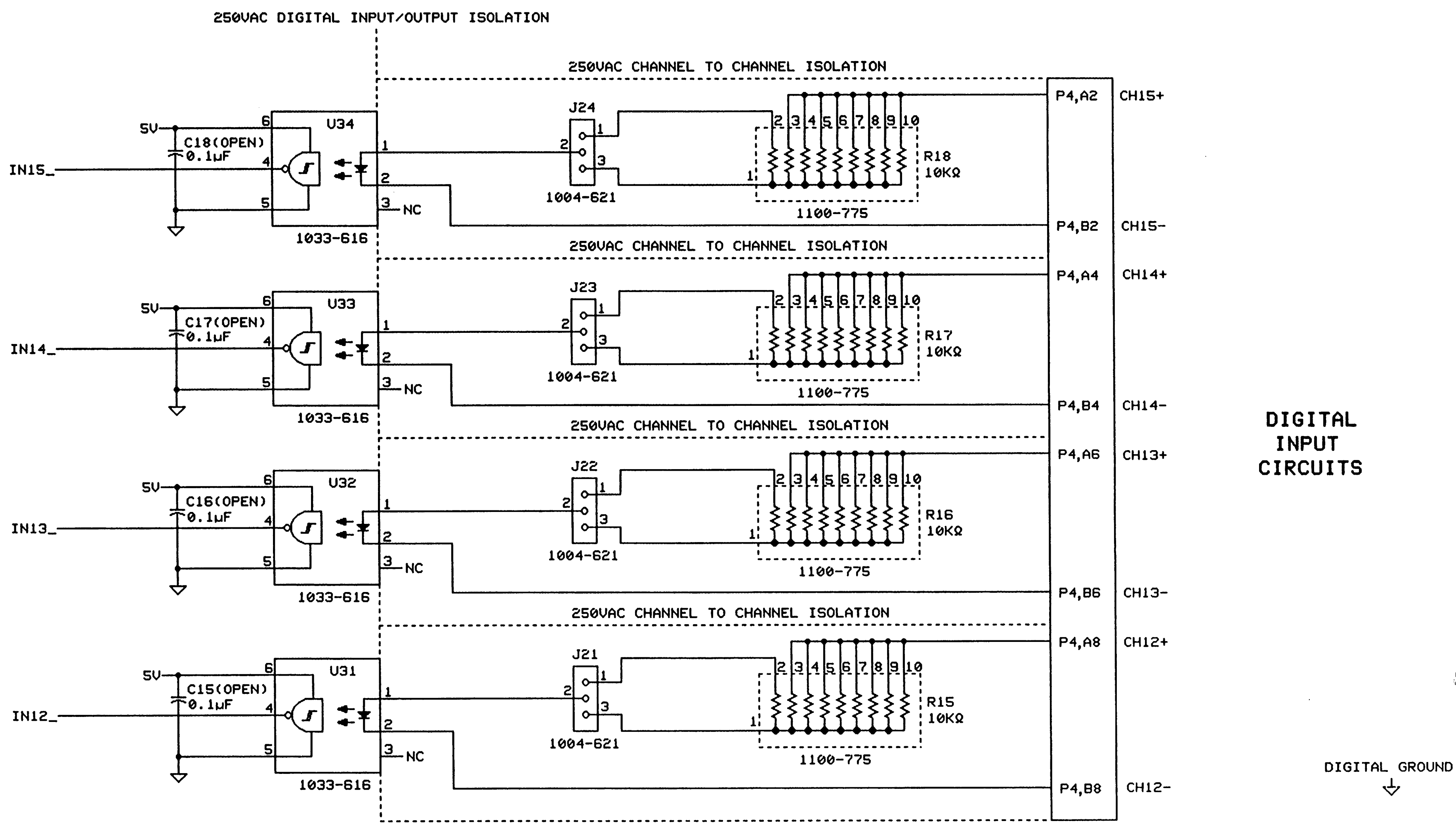
DIGITAL INPUT CIRCUITS

AcroMag MIXOM, MICH.	27 OCT 92	A	10317	TAV	ATS	TH
	30 MAY 91	-	——	TAV	ATS	—
	DATE	REV	CO	DR	ENG	CLP

TITLE: ISOLATED DIGITAL I/O BOARD

SIZE	SERIES	SHEET	DRAWING	REV
D DWG	AVME944x	11OF13	4501-129	A


DIGITAL INPUT CIRCUITS
250VAC DIGITAL INPUT/OUTPUT ISOLATION
250VAC CHANNEL TO CHANNEL ISOLATION
R20,270Ω
1100-635
5V
NC
IN15
IN14
IN13
IN12
IN11
IN10
IN09
IN08
P7,4
P7,9
P7,5
P7,8
P7,3
P7,7
P7,2
P7,6
P7,1
1004-626
C14 0.1µF
C13 0.1µF
C12(OPEN) 0.1µF
C11(OPEN) 0.1µF
U30
U29
U28
U27
1033-616
J20
J19
J18
J17
1004-621
R14 10KΩ
R13 10KΩ
R12 10KΩ
R11 10KΩ
1100-775
P4,A10 CH11+
P4,B10 CH11-
P4,A12 CH10+
P4,B12 CH10-
P4,A14 CH9+
P4,B14 CH9-
P4,A16 CH8+
P4,B16 CH8-
DIGITAL GROUND
AcroMag WIXOM, MICH.
27 OCT 92 A 10317 TAV ATS TH
30 MAY 91 - TAV ATS
DATE RV C0 DR ENG CLP
TITLE ISOLATED DIGITAL I/O BOARD
SIZE D DWG
SERIES AVME944x
SHEET 12OF13
DRAWING 4501-129
REV A

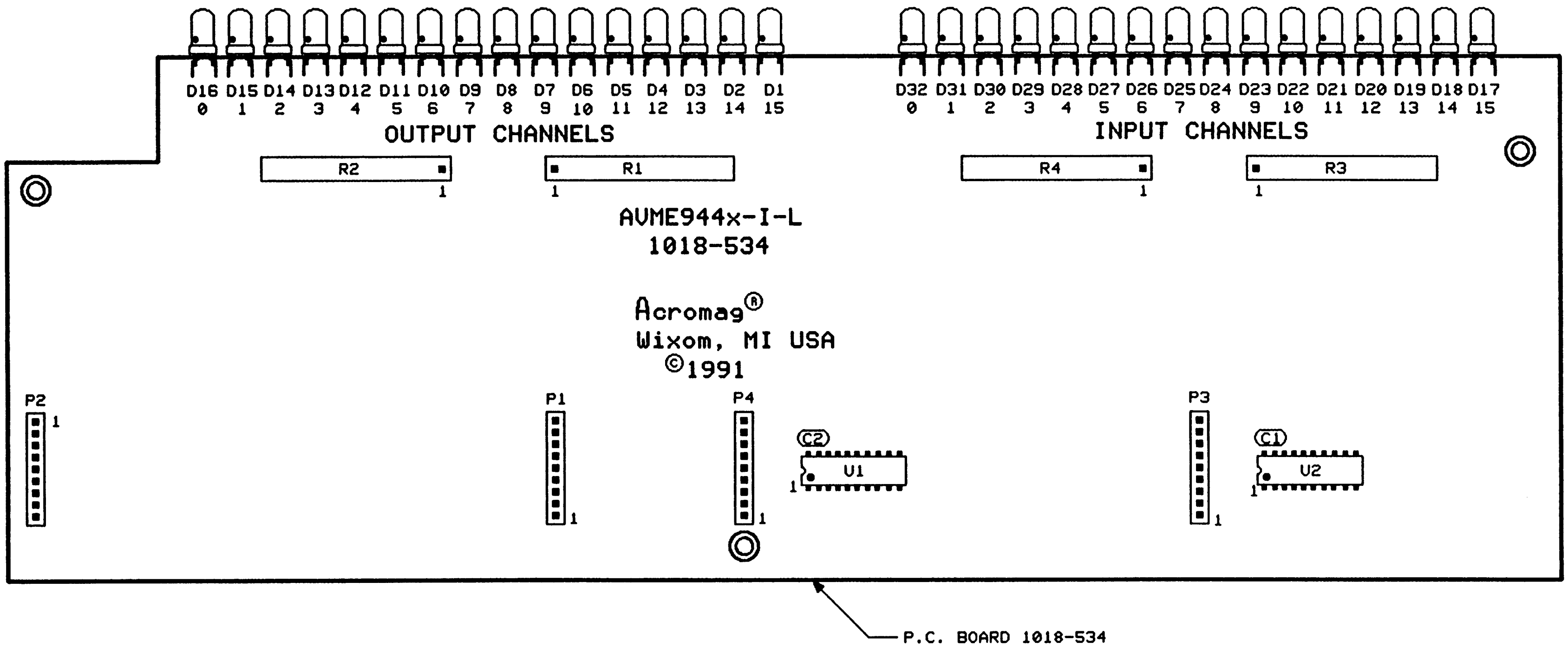


DIGITAL INPUT CIRCUITS

AcroMag® WIXOM, MICH.	27 OCT 92	A	10317	TAV	ATS	TH
	30 MAY 91	-	—	TAV	ATS	—
	DATE	REV	EO	DR	ENG	CLP

TITLE: ISOLATED DIGITAL I/O BOARD

SIZE	SERIES	SHEET	DRAWING	REV
D DWG	AVME944x	13 OF 13	4501-129	A



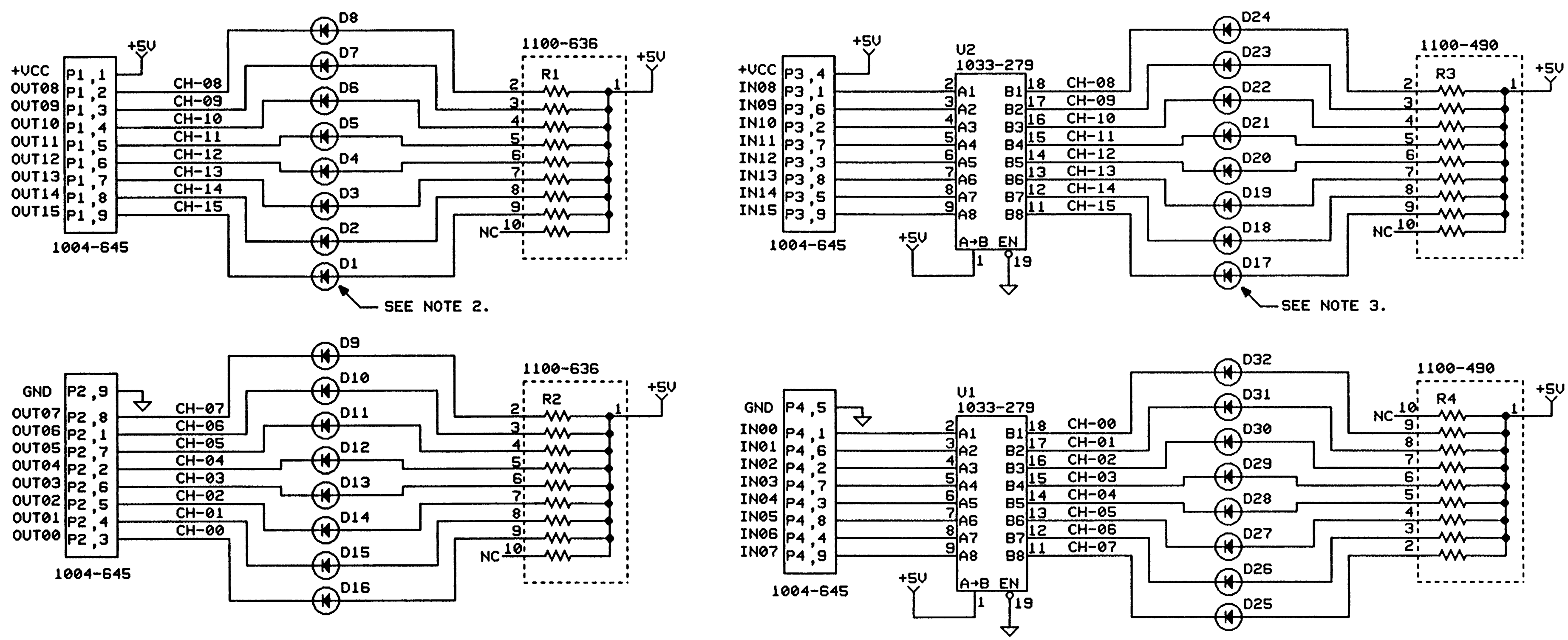
Acromag® WIXOM, MICH.

28 OCT 91 — — TAV ATS —

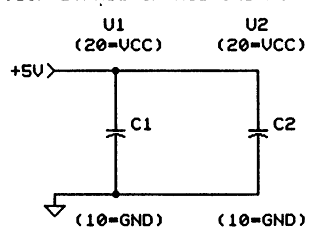
DATE RV CB DR ENG ELP

TITLE: LED OPTION BOARD SCHEMATIC AND PARTS LOCATION

SIZE: D DWG | SERIES: AVME944x | SHEET: 1 OF 2 | DRAWING: 4501-136 | REV



0.1UF BYPASS CAPACITORS FOR IC'S



NOTES:

1. ALL SEVEN DIGIT PART NUMBERS ARE ACROMAG PART NUMBERS.
2. D1 THROUGH D16 ARE ACROMAG 1001-198.
3. D17 THROUGH D32 ARE ACROMAG 1001-199.
4. PRINTED CIRCUIT BOARD IS 1018-534.

USED LAST: P4,U2,D32,C2,R4

AcroMag® WIXOM, MICH.

DATE	RV	CE	DR	ENG	CLP
28 OCT 91	-	——	JOM	ATS	—

TITLE: LED OPTION BOARD SCHEMATIC AND PARTS LOCATION

SIZE	SERIES	SHEET	DRAWING	REV
D DWG	AVME944x	2 OF 2	4501-136	

APPENDIX A

A.0 CABLE AND TERMINATION PANELS

A.1 CABLE: MODEL 9944-x

Type: Ribbon Cable, 64 wire (Header - Header)

This cable connects the 6985-16Dx termination panel to the AVME944x board. The length of the cable in feet is indicated by the "x" in the model number (9944-x), 12 feet maximum. It is recommended that this length be kept to a minimum to reduce noise pickup and power loss (especially important for output channels, since their currents can reach 1 Amp DC).

Part numbers are given below for the various cable components. Use these references if you wish to assemble your own cables.

MODEL: 9944-x

Application..Use to connect 6985-16Dx termination panel to the AVME944x board (both have 64 pin connectors).
Cable..64 wire flat ribbon cable, 28 gauge. Acromag Part 2002-210 (3M Type C3365/64 or equivalent).
Length...Last field in part number designates length in feet, specified by user (12 feet maximum).
Headers (Both Ends)...............................64-pin header, female, includes strain relief.
Header: Acromag Part 1004-686
(Panduit Type 120-064-435 or equiv.).
Strain Relief*:* Acromag Part 1004-682
(Panduit Type 120-000-032 or equiv.).
Keying...Headers, both ends, have polarizing key to prevent improper installation.
Schematic and Mech. Dimensions......... See Drawing 4501-135.
Shipping Weight...................................1.0 pounds (0.5Kg) packed.

A.2 TERMINATION PANELS: MODELS 6985-16DI AND 6985-16DO

Type: Termination Panels For AVME944x Board

The 6985-16DI (6985-16DO) panel facilitates the connection of up to 16 field input (output) signals and connects to the AVME944x board via a flat ribbon cable (Model 9944-x). Field signals are accessed via screw terminal strips.

Optionally, the user may connect a +5 to +55V DC supply to the B+ and B- power (screw) terminals to provide a common supply reference for I/O channels (e.g. a +5V DC supply would be useful for interfacing to TTL signals as shown in Figure 2.7). The panels have slots to add pull-up/down resistors (or jumpers) or protection diodes from each channel to the B+ and B- terminals. See Drawing 4501-126: 6985-16Dx Schematic and Part Location Drawing for specifics. Typical input and output channel configurations are shown in Figures 2.4 and 2.6, respectively. If the application requires that channel to channel isolation be maintained, then do not compromise this by making connections to a common supply (i.e. the B+ and B- terminals).

Before connecting the 6985-16Dx termination panel to the AVME944x board, connect a wire from chassis ground to the ground (GND) screw terminal on the panel (see Drawing 4501-127: 6985-16Dx Mounting, Clearance & Electrical Connections). This wire ties the input/output transient protection circuitry to ground.

MODELS: 6985-16DI and 6985-16DO

FEATURES:

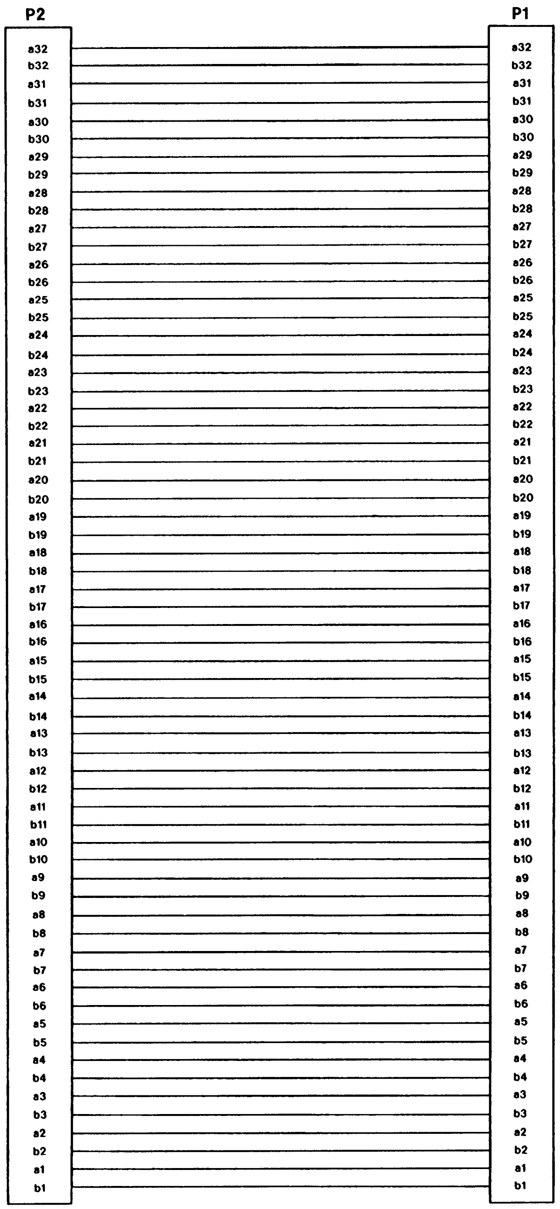
Digital Input Channels...........................Up to 16 channels with 6985-16DI.
Digital Output Channels........................Up to 16 channels with 6985-16DO.
Wiring Connections..............................See Drawing 4501-127.
Power..Optional user supply terminals (B+ andB-); do not use if channel to channel isolation is required. Supply Range: +5 to +55V DC. (3 Amps maximum for pc board foil traces)
Power On LED......................................Illuminates if a +5 to +55V DC supply is connected to the B+ and B- power (screw) terminals.
User Configurable Panel Circuits...........See Drawing 4501-126. Slots to add pull-up/down resistors (or jumpers) or protection diodes from each channel to the B+ and B- terminals.
Isolation..250VAC or 354V DC Between all digital I/O channels. 250VAC or 354V DC Between all digital I/O channels and the ground terminal.
Input/Output Transient Protection..........See Drawing 4501-127. Connect a wire from chassis ground to the ground (GND) screw terminal on the panel.

PHYSICAL CHARACTERISTICS:

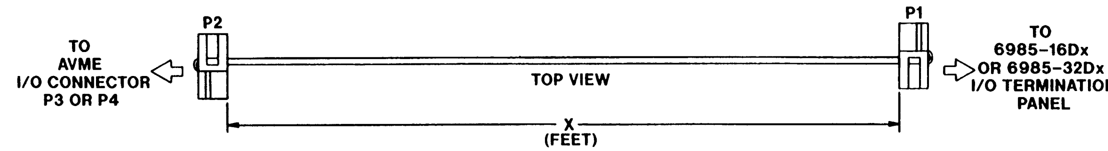
Shipping Weight.....................................1.25 pounds (0.6Kg) packed.
Mounting..Surface mounting. Leave sufficient space around the termination panel for wiring.
Mounting Hardware.............................. .The termination panel is supplied with 0.375 inch standoffs. All standoffs should be secured using No. 6 hardware to provide maximum physical strength.
Field/Power Wiring................................Terminal blocks with screw clamps. Wire range 14 to 26 AWG.
Connections to AVME944x....................P1; Panduit No. 100-532-033; Type B Male Connector, rows A & B equipped, even pins only (32 pins total). Use Acromag 9944-x cable (keyed) to connect panel to VME board. Keep cable short to reduce power loss and noise.
Mechanical Dimensions.........................See Drawing 4501-127.
Printed Circuit Board..............................Military grade FR-4 epoxy glass circuit board. Thickness: 0.063 inches.

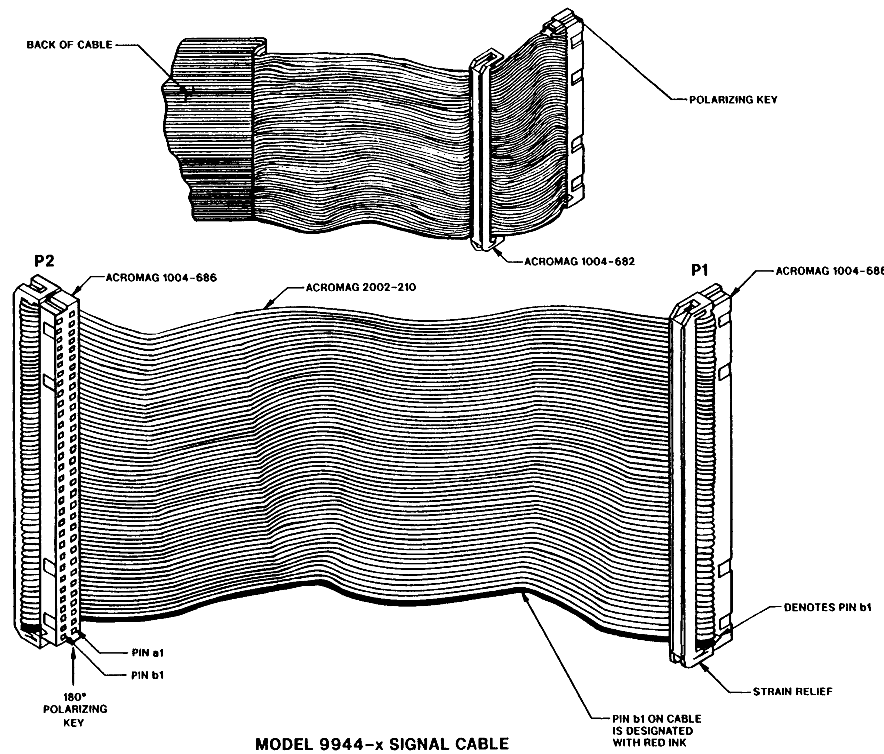
OPERATING CONDITIONS:

Operating Temperature..........................0 to 70 deg. C.
Storage Temperature.............................-25 to +85 deg. C.



MODEL 9944-x SCHEMATIC





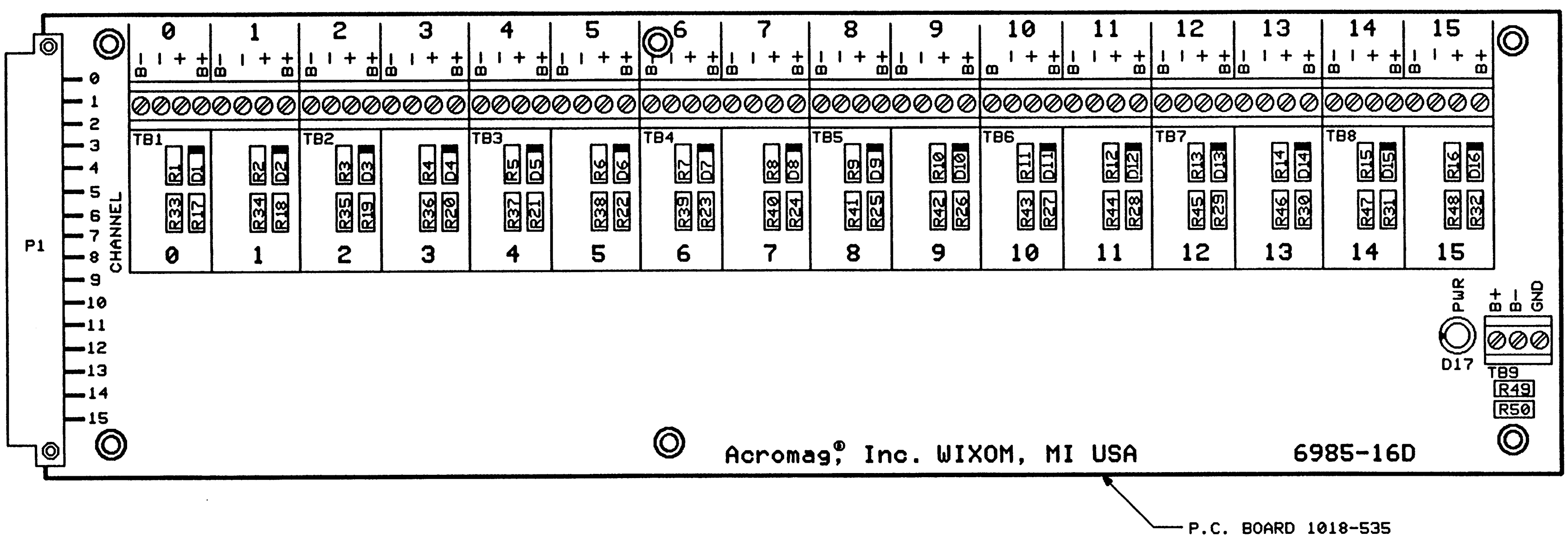
MODEL 9944-x SIGNAL CABLE
FRONT VIEW

Acromag® WIXOM, MICH.	18 DEC 92	A	10362	TV	ATS	TH
	8 NOV 91	–	——	TV	ATS	—
	DATE	REV	CO	DR	ENG	CLP

TITLE CABLE: MODEL 9944-x

SIZE	SERIES	SHEET	DRAWING	REV
D DWG	AVME	1 OF 1	4501-135	A

3600-026

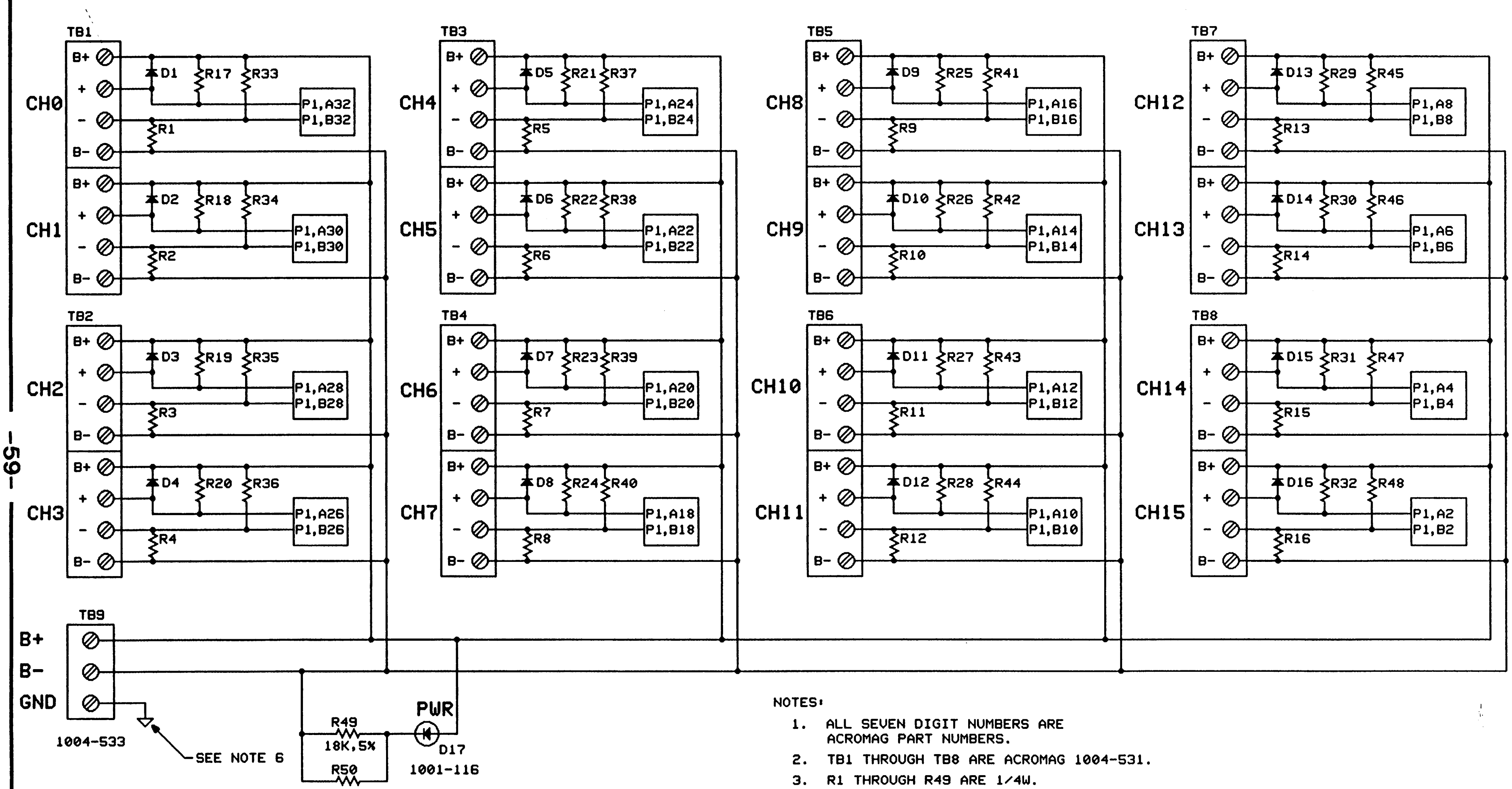


AcroMag® WIXOM, MICH.

12 NOV 91 TAV ATS

TITLE 6985-16Dx TERMINATION PANEL SCHEMATIC AND PARTS LOCATION

SIZE D DWG | SERIES AVME | SHEET 1 OF 2 | DRAWING 4501-126 | REV



NOTES:

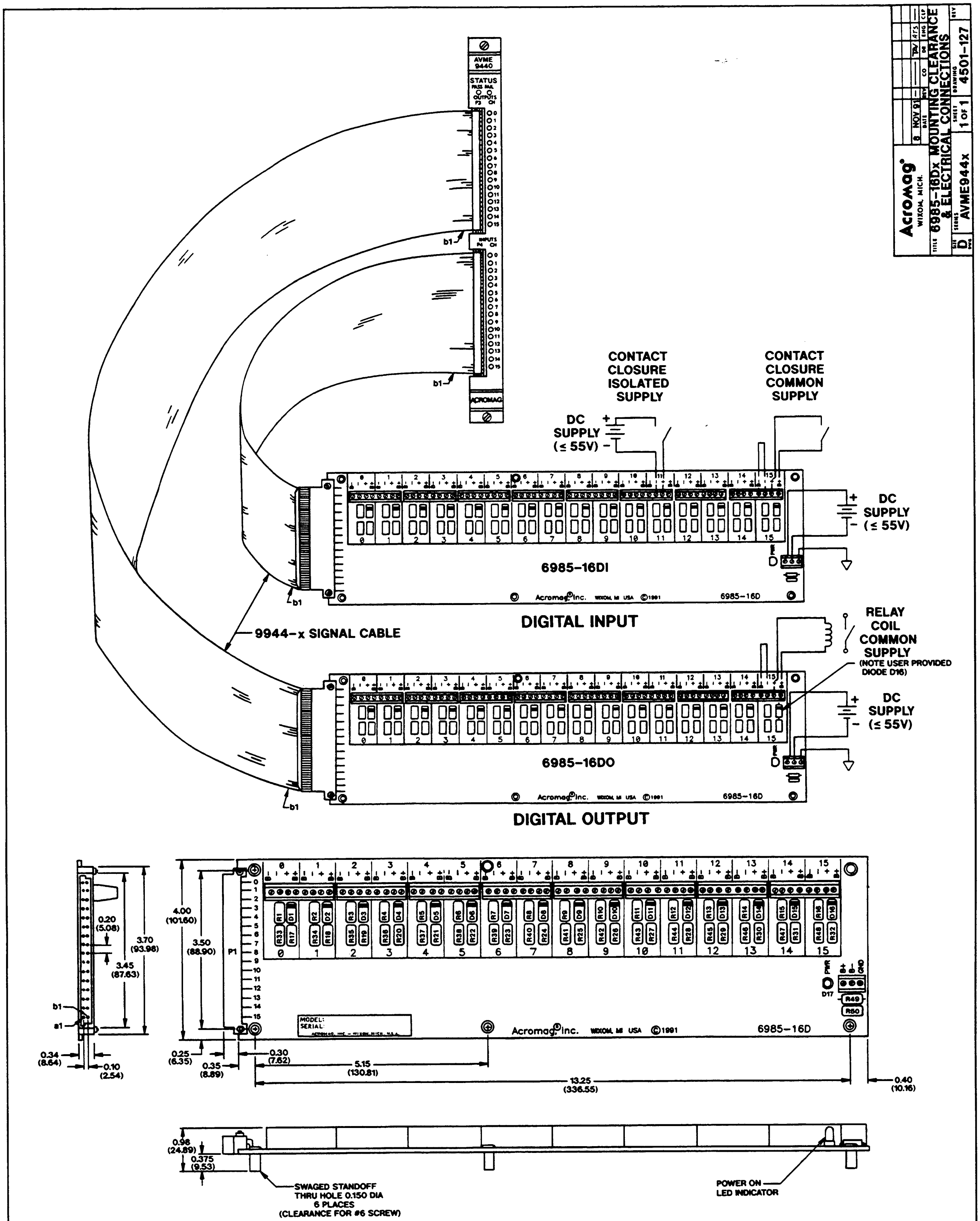
1. ALL SEVEN DIGIT NUMBERS ARE ACROMAG PART NUMBERS.
2. TB1 THROUGH TB8 ARE ACROMAG 1004-531.
3. R1 THROUGH R49 ARE 1/4W.
4. R50 IS OPTIONAL.
5. D1 THROUGH D16 ACCEPT TS2 LEADS.
6. EACH CHANNELS' (+) AND (-) INPUT CONTAINS A 0.064" SPARK GAP AND A SLOT FOR A SPARK ARRESTER TO GND OF TB9.
7. P.C. BOARD IS 1018-535.

AcroMag® WIXOM, MICH.

12 NOV 91	-	——	JOM	ATS	—
DATE	RV	CB	DR	ENG	CLP

TITLE 6985-16Dx TERMINATION PANEL SCHEMATIC AND PARTS LOCATION

SIZE	SERIES	SHEET	DRAWING	REV
D DWG	AVME	2 OF 2	4501-126	



6985-16Dx TERMINATION PANEL MOUNTING, CLEARANCE AND ELECTRICAL CONNECTIONS

DIMENSIONS: INCHES (MILLIMETERS)
TOLERANCE: ± 0.020 (± 0.5)